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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	ELLIS	Group: Unknown
Serial No.:	10/684,657	Examiner: Unknown
Filed:	October 15, 2003	
For:	GLOBAL NETWORK COMPUTERS	

PETITION FOR FILING DATE

Attention: Office of Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice of Incomplete Application mailed March 29, 2004, the due date for response being June 1, 2004 in view of the intervening weekend and holiday, the Applicant submits the present Petition to obtain a filing date of October 15, 2003 for the subject application.

On March 29, 2004, the United States Patent and Trademark Office issued a Notice of Incomplete Application indicating that a filing date was not accorded to the subject application due to the absence in the initial papers of a complete specification as prescribed by 35 U.S.C. § 112. It is respectfully submitted that a complete specification was in fact submitted on October 15, 2003. The Applicant, an independent sole inventor, filed his application without the assistance of a patent practitioner. He filed the following papers:

1. Utility Patent Application Transmittal (Form PTO/SB/05) **referencing provisional application 60/418,177**

2. Declaration for Utility or Design Patent Application (Form PTO/SB/01) **referencing provisional application 60/418,177**

3. Declaration for Utility or Design Application Using an Application Data Sheet (Form PTO/SB/01A) **referencing provisional application 60/418,177**

4. Statement Claiming Small Entity Status (Form PTO/SB/09)

5. Fee Transmittal (Form PTO/SB/17)

6. A **return receipt postcard** on which the Applicant wrote:

> PTO Stamp indicates receipt of a non-provisional Utility Patent Application titled "Global Network Computers" filed October 15, 2003 by Frampton E. Ellis, III, with new page 91 only **(to be incorporated with 90 pages of specification and 31 sheets of 31 Figures of referenced provisional patent application No. 60/418,177 filed 10/15/02 by F. Ellis)**, together with filing fee check for $385.00.

7. A single sheet of paper numbered as page 91, reciting two claims.

Clearly, the Applicant intended to incorporate by reference the entire specification of provisional application 60/418,177, appending to that incorporated specification two claims on the submitted single sheet of paper numbered 91. While the Applicant's manner of filing may have been unconventional, it is respectfully submitted that the Applicant filed a complete specification as prescribed by 35 U.S.C. § 112. Submitted along with this Petition are a copy of the filed papers, a copy of the stamped postcard returned by the Patent Office, and a copy of the incorporated provisional application 60/418,177.

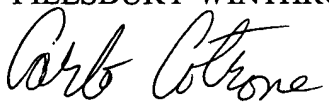
In addition, the Applicant now submits (1) a Substitute Specification, (2) Informal Drawings, (3) an executed Declaration and Power of Attorney, and (4) an Application Data Sheet. The Applicant will later prepare and submit Formal Drawings.

In view of the foregoing, it is respectfully requested that this petition be granted, and that a filing date of October 15, 2003 be accorded to the subject application.

The Petition Fee in the amount of $130 is enclosed. Along with this Petition, the Applicant has submitted a request that the Petition Fee be refunded to our Deposit Account No. 03-3975.

Respectfully submitted,

PILLSBURY WINTHROP LLP



CARLO M. COTRONE
Reg. No. 48715
Tel. No. (703) 905-2041
Fax No. (703) 905-2500

Date: June 1, 2004
P.O. Box 10500
McLean, VA 22102
(703) 905-2000

Attorney Docket No. 081498-0306614 *PATENT*
Client Reference: GNC26US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: FRAMPTON E ELLIS

Application No.:	10/684,657	Confirmation No:
Filed:	October 15, 2003	Group No.:
		Examiner:

For: GLOBAL NETWORK COMPUTERS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICATION DATA SHEET
37 C.F.R. § 1.76

BIBLIOGRAPHIC DATA

1. Applicant information

First applicant: FRAMPTON E ELLIS
Citizenship: USA
Residence: Jasper, FL 32052

2. Correspondence information

Correspondence for this application should be addressed as follows:

Customer No.: 00909

3. Application information

Title of Invention: GLOBAL NETWORK COMPUTERS

Docket number assigned to this application: 081498-0306614
Suggested Classification: Class:
Subclass:
Technology Center to which subject matter is assigned:

Total number of drawing sheets: 31
Type of application: Utility
Application is to be published. Suggested drawing figure for publication:

Secrecy order under § 5.2:

This application does not disclose subject matter of an application which is under a secrecy order pursuant to § 5.2.

4. Representative information

The following have a power of attorney or authorization of agent in this application:

Customer No.: 00909 Customer No.: 00909

5. Domestic Priority information

Domestic priority for this application is claimed as follows:

35 U.S.C. § 120:

Application No.: 60/418,177
Filed: October 15, 2002
Status: abandoned
Relationship: priority

Application No.: PCT/US02/29227
Filed: September 16, 2002
Status: pending
Relationship: CIP parent

Application No.: 60/322,474
Filed: September 17, 2001
Status: abandoned
Relationship: priority for PCT/US02/29227

Application No.: 60/323,701
Filed: September 21, 2001
Status: abandoned
Relationship: priority for PCT/US02/29227

Application No.: 09/935,779
Filed: August 24, 2001
Status: pending
Relationship: CIP parent

Application No.: 60/308,826
Filed: 1 August 2001
Status: abandoned
Relationship: priority for 09/935,779

Application No.: 60/227,660
Filed: 25 August 2000
Status: abandoned
Relationship: priority for 09/935,779

Application No.: 09/571,558
Filed: 16 May 2000
Status: pending
Relationship: CIP parent of 09/935,779

Application No.: 60/136,759
Filed: 28 May 1999
Status: abandoned
Relationship: priority for 09/571,558

Application No.: 60/135,852
Filed: 24 May 1999
Status: abandoned
Relationship: priority for 09/571,558

Application No.: 60/135,851
Filed: 24 May 1999
Status: abandoned
Relationship: priority for 09/571,558

Application No.: 09/315,026
Filed: 20 May 1999
Status: pending
Relationship: CIP parent of 09/935,779, CIP parent of 09/571,558

Application No.: 60/134,552
Filed: 17 May 1999
Status: abandoned
Relationship: priority for 09/571,558, 09/315,026

Application No.: PCT/US98/27058
Filed: 17 December 1998
Status: abandoned
Relationship: CIP parent of 09/315,026

Application No.: 09/213,875
Filed: 17 December 1998
Status: patented
Relationship: CIP parent of 09/935,779, CIP parent of 09/571,558, CIP parent of 09/315,026

Application No.: 60/088,459
Filed: 8 June 1998
Status: abandoned
Relationship: priority for 09/315,026

Application No.: 60/087,587
Filed: 1 June 1998
Status: abandoned
Relationship: priority for 09/315,026

Application No.: 60/086,948
Filed: 27 May 1998
Status: abandoned
Relationship: priority for 09/315,026

Application No.: 60/086,516
Filed: 22 May 1998
Status: abandoned
Relationship: priority for 09/315,026, 09/085,755

Application No.: 60/086,588
Filed: 22 May 1998
Status: abandoned
Relationship: priority for 09/315,026, 09/085,755

Application No.: 09/085,755
Filed: 21 May 1998
Status: pending
Relationship: CIP parent of 09/935,779, CIP parent of 09/571,558, CIP parent of 09/315,026

Application No.: 60/068,366
Filed: 19 December 1997
Status: abandoned
Relationship: priority for 09/213,875, PCT/US98/27058, 09/085,755

Application No.: PCT/US97/21812
Filed: 28 November 1997
Status: abandoned
Relationship: CIP parent of 09/315,026, CIP parent of 09/085,755

Application No.: 08/980,058
Filed: 26 November 1997
Status: patented
Relationship: CIP parent of 09/213,875, CIP parent of PCT/US97/21812, CIP parent of 09/085,755, CIP parent of 09/935,779

Application No.: 60/066,415
Filed: 24 November 1997
Status: abandoned
Relationship: priority for 08/980,058, PCT/US97/21812, 09/085,755

Application No.: 60/066,313
Filed: 21 November 1997
Status: abandoned
Relationship: priority for 08/980,058, PCT/US97/21812, 09/085,755

Application No.: 60/033,871
Filed: 20 December 1996
Status: abandoned
Relationship: priority for 08/980,058, PCT/US97/21812

Application No.: 60/032,207
Filed: 2 December 1996
Status: abandoned
Relationship: priority for 08/980,058, PCT/US97/21812

Application No.: 60/031,855
Filed: 29 November 1996
Status: abandoned
Relationship: priority for 08/980,058, PCT/US97/21812

6. Assignee information

The assignee(s) of this application is/are:

Date: June 1, 2004

Signature of Practitioner
Carlo M. Cotrone
Registration No. 48715
(703) 905-2041

PILLSBURY WINTHROP LLP
P.O. Box 10500
McLean, VA 22102
Customer No. 00909

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

ELLIS

Group Art Unit:

Appln. No.: 10/684,657

Examiner:

Filed: October 15, 2003

FOR: GLOBAL NETWORK COMPUTERS

* * * * *

June 1, 2004

REQUEST FOR REFUND UNDER 37 C.F.R. § 1.26

Mail Stop 16
Director of the US Patent and Trademark Office
Alexandria, VA 22313-1450

Sir:

The undersigned respectfully requests that Deposit Account No. 03-3975 be credited in the amount of $130.00.

A Petition for Filing Date was filed on June 1, 2004 in response to a Notice of Incomplete Application mailed March 29, 2004. The Petition authorized the charging of Deposit Account No. 03-3975 in the amount of $130.00.

The Notice of Incomplete Application provided that "[i]f the petition states that the application is entitled to a filing date, a request for a refund of the petition fee may be included in the petition." Because the Petitioner made such a statement, this Request for Refund is proper.

The undersigned respectfully requests that Deposit Account No. 03-3975 be credited in the amount of $130.00.

Respectfully submitted,

PILLSBURY WINTHROP LLP

By

CARLO M. COTRONE
Reg. No. 48715
Tel. No.: (703) 905-2041
Fax No.: (703) 905-2500

CMC
P.O. Box 10500
McLean, VA 22102
(703) 905-2000

IFW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/684,657	10/15/2003	Frampton Erroll Ellis III	GNC26US

CONFIRMATION NO. 3226

00909
PILLSBURY WINTHROP, LLP
P.O. BOX 10500
MCLEAN, VA 22102

FORMALITIES LETTER

OC000000012205143

Date Mailed: 03/29/2004

NOTICE OF INCOMPLETE NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

A filing date has NOT been accorded to the above-identified application papers for the reason(s) indicated below.

All of the items noted below **and a newly executed oath or declaration covering the items must** be submitted within **TWO MONTHS** of the date of this Notice, unless otherwise indicated, or proceedings on the application will be terminated *(37 CFR 1.53(e))*. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

The filing date will be the date of receipt of all items required below, unless otherwise indicated. Any assertions that the item(s) required below were submitted, or are not necessary for a filing date, must be by way of petition directed to the attention of the Office of Petitions accompanied by the $130.00 petition fee *(37 CFR 1.17(h))*. If the petition states that the application is entitled to a filing date, a request for a refund of the petition fee may be included in the petition. Petitions should be mailed to: Mail Stop Petitions, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

- The specification is missing.
  A complete specification as prescribed by 35 U.S.C. 112 is required.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

J Stokes

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

[X] Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete if Known	
Application Number	10/684,657
Filing Date	October 15, 2003
First Named Inventor	ELLIS E FRAMPTON
Examiner Name	Unknown
Art Unit	
Attorney Docket No.	081498-0306614

METHOD OF PAYMENT *(check all that apply)*

[ ] Check [ ] Credit card [ ] Money Order [ ] Other [ ] None

[X] Deposit Account:

Deposit Account Number: 033975

Deposit Account Name: PILLSBURY WINTHROP LLP

The Director is authorized to: *(check all that apply)*

[X] Charge fee(s) indicated below [X] Credit any overpayments

[X] Charge any additional fee(s) or any underpayment of fee(s)

[ ] Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X =
Independent Claims		- 3** =		X =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	130.00
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Carlo M. Cotrone	Registration No. *(Attorney/Agent)*	48715	Telephone	(703) 905-2041
Signature	Carlo Cotrone			Date	June 1, 2004

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

FOR UTILITY ORIGINAL DECLARATION

RULE 63 (37 C.F.R. 1.63) DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the **INVENTION ENTITLED GLOBAL NETWORK COMPUTERS**, the specification of which was filed on October 15, 2003 as U.S. Application No. 10/684,657.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)

Number	Country	Filed	Date First Laid Open Or Published	Date Patented or Granted	Priority Claimed

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S)

Application Number	Filed	Status pending, abandoned, patented	Priority Claimed
60/418,177	15 October 2002	abandoned	Yes
PCT/US02/29227	16 September 2002	pending	Yes
60/322,474	17 September 2001	abandoned	Yes
60/323,701	21 September 2001	abandoned	Yes
09/935,779	24 August 2001	pending	Yes
60/308,826	1 August 2001	abandoned	Yes
60/227,660	25 August 2000	abandoned	Yes
09/571,558	16 May 2000	pending	Yes
60/136,759	28 May 1999	abandoned	Yes
60/135,852	24 May 1999	abandoned	Yes
60/135,851	24 May 1999	abandoned	Yes
09/315,026	20 May 1999	pending	Yes
60/134,552	17 May 1999	abandoned	Yes
PCT/US98/27058	17 December 1998	abandoned	Yes
09/213,875	17 December 1998	patented	Yes
60/088,459	8 June 1998	abandoned	Yes
60/087,587	1 June 1998	abandoned	Yes
60/086,948	27 May 1998	abandoned	Yes
60/086,516	22 May 1998	abandoned	Yes
60/086,588	22 May 1998	abandoned	Yes
09/085,755	21 May 1998	pending	Yes
60/068,366	19 December 1997	abandoned	Yes
PCT/US97/21812	28 November 1997	abandoned	Yes
08/980,058	26 November 1997	patented	Yes
60/066,415	24 November 1997	abandoned	Yes
60/066,313	21 November 1997	abandoned	Yes
60/033,871	20 December 1996	abandoned	Yes
60/032,207	2 December 1996	abandoned	Yes
60/031,855	29 November 1996	abandoned	Yes

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

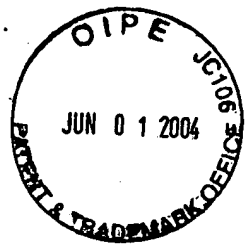
And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, (to whom all communications are to be directed), and persons of that firm who are associated with USPTO Customer No. 00909 individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete from that Customer No. names of persons no longer with their firm, to add new persons of their Firm to that Customer No., and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or an attorney of that Firm in writing to the contrary.

Power of Attorney to Customer Number 00909

INVENTOR'S SIGNATURE: _____ **Date:** May 26, 2004

Name	FRAMPTON	E	ELLIS
	First	Middle Initial	Family Name
Residence	Jasper	FLA	USA
	City	State/Foreign Country	Country of Citizenship
Mailing Address	P.O. Box 1029, Jasper, FL 32052		

Atty. Dkt. No. 081498-0306614



PTO Stamp indicates receipt of Non-provisional Utility Patent Application titled "Global Network Computers" filed on October 15, 2003 by Frampton E. Ellis, III, with New page 91 only (to be incorporated with 90 pages of specification and 31 sheets of 31 Figures of reprenced provisional patent application No. 60/418,177 filed 10/15/02 by F. Ellis), together with ~~filing fee check~~ $385. (Docket No: GATC26 US)

PTO/SB/05 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Please type a plus sign (+) inside this box → ☐

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	GNC26US
First Inventor	Frampton E. Ellis
Title	Global Network Computers
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [Total Pages 91]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 31]
5. Oath or Declaration [Total Pages 3]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [ ] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [ ] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Nonpublication Request under 35 U.S.C 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other:

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. 60/418,177

Prior application information Examiner _____ Group Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label [redacted] or [X] Correspondence address below

Name	Frampton Ellis				
Address	P.O. Box 1029				
City	Jasper	State	Florida	Zip Code	32052
Country	USA	Telephone	386.792.2636	Fax	792-2393

Name (Print/Type)	Frampton Ellis	Registration No. (Attorney/Agent)	
Signature		Date	10/15/03

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington DC 20231

PTO/SB/01 (10-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	GNC26US
First Named Inventor	Frampton E. Ellis
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Art Unit	
Examiner Name	

As the below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

GLOBAL NETWORK COMPUTERS

(Title of the Invention)

the specification of which

[ ] is attached hereto

OR

[X] was filed on (MM/DD/YYYY) October 15, 2002 as United States Application Number or PCT International Application Number 60/418,177 and was amended on (MM/DD/YYYY) Oct. 15, 2003 (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

PTO/SB/01A (10-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	GLOBAL NETWORK COMPUTERS

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☐ The attached application, or

☒ Application No. 60/418,177, filed on October 15, 2002

☒ as amended on October 15, 2003 (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

All statements made herein of my/own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Frampton E. Ellis, III

Signature: _____ Citizen of: USA

Inventor two: _____

Signature: _____ Citizen of: _____

Inventor three: _____

Signature: _____ Citizen of: _____

Inventor four: _____

Signature: _____ Citizen of: _____

☐ Additional inventors are being named on _____ additional form(s) attached hereto.

Burden Hour Statement: This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is used by the public to file (and the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 1 minute to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

NAME OF SOLE OR FIRST INVENTOR :	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any]) Frampton Erroll		Family Name or Surname Ellis, III	
Inventor's Signature			Date 10/15/03
Residence: City Jasper	State Florida	Country USA	Citizenship USA
Mailing Address P.O. Box 1029			
City Jasper	State Florida	ZIP 32052	Country USA
NAME OF SECOND INVENTOR:	☐ A petition has been filed for this unsigned inventor		
Given Name (first and middle [if any])		Family Name or Surname	
Inventor's Signature			Date
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	ZIP	Country

☐ Additional inventors are being named on the ___supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

PTO/SB/01 (10-01)
Approved for use through 10/31/2002 OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION — Utility or Design Patent Application

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] OR [X] Correspondence address below

Name: Frampton Ellis

Address: P.O. Box 1029

City: Jasper | State: Florida | ZIP: 32052

Country: USA | Telephone: 386.792.2636 | Fax: 792.2393

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(b))—INDEPENDENT INVENTOR	Docket Number (Optional)

Applicant, Patentee, or Identifier: Frampton E. ELLIS, III

Application or Patent No.: —

Filed or Issued: —

Title: Global Network Computers

As a below named inventor, I hereby state that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office described in:

- [X] the specification filed herewith with title as listed above.
- [ ] the application identified above.
- [ ] the patent identified above.

I have not assigned, granted, conveyed, or licensed, and am under no obligation under contract or law to assign, grant, convey, or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- [X] No such person, concern, or organization exists.
- [ ] Each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern, or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

Frampton E. ELLIS III		
NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
Signature of inventor	Signature of inventor	Signature of inventor
Date 8/25/00	Date	Date

I Claim:

1. A microchip comprising:

a plurality of dies, each made by a separate fabrication process and assembled into a package with the separate die sections connected directly.

2. The microchip according to claim 1, wherein the separate die sections are connected by interconnects that are widened compared to the ciruits of the die.

PTO/SB/17 (11-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($)

Complete If Known	
Application Number	
Filing Date	October 15, 2003
First Named Inventor	Frampton Ellis
Examiner Name	
Group Art Unit	
Attorney Docket No.	GNC26US

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account.

Deposit Account Number:
Deposit Account Name:

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments
☐ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, except for the filing fee
to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	385
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 385

2 EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims	2 - 20** =		x	=
Independent Claims	1 - 3** =		x	=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($)

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Frampton Ellis	Registration No. (Attorney/Agent)		Telephone	386.792.2636
Signature				Date	10/15/03

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

D Pender to Inspect 10/27/03

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

10/16/2002 BSAYASI1 00000175 60418177
01 FC:2005 80.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
Washington, DC 20231
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 5268

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
60/418,177	10/15/2002 RULE			GNCZ 26 PA

APPLICANTS

Frampton E. Ellis, Arlington, VA;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
** 11/08/2002

Foreign Priority claimed	35 USC 119 (a-d) conditions met	Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☐ no	☐ yes ☐ no ☐ Met after Allowance	Examiner's Signature Initials	VA	31		

ADDRESS

F. E. ELLIS
B2
2895 South Abingdon St.
Arlington ,VA 22206-1331

TITLE

Global network computers

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
80	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

A(P)

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

INVENTOR(S)		
Given Name (first and middle (if any))	Family Name or Surname	Residence (City and either State or Foreign Country)
Frampton E.	ELLIS	Arlington, Virginia

No Additional inventors are being named on the ___ separately numbered sheets attached hereto

TITLE OF THE INVENTION (280 characters max)

Global Network Computers

CORRESPONDENCE ADDRESS

Direct all correspondence to:

Customer Number ____ → Place Customer Number Bar Code Label here

OR Type Customer Number here

X Firm or Individual Name: F.E. ELLIS

Address: 2895 South Abingdon St. #B2

Address:

City: Arlington | State: VA | ZIP: 22206-1331

Country: USA | Telephone: 703.931-6111 | Fax: 703.931-1116

ENCLOSED APPLICATION PARTS (check all that apply)

X Specification Number of Pages: 90 — X Small Entity Statement

X Drawing(s) Number of Sheets: 31 Figures 31 — Other (specify):

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

X A check or money order is enclosed to cover the filing fees — FILING FEE AMOUNT ($)

___ The Commissioner is hereby authorized to charge filing ___ fees or credit any overpayment to Deposit Account Number: ____

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

X No.

___ Yes, the name of the U.S. Government agency and the Government contract number are: ____

Respectfully submitted,

SIGNATURE: [signature] Date: 10/15/02

TYPED or PRINTED NAME: Frampton E. Ellis — REGISTRATION NO. (if appropriate): ____

TELEPHONE: 703.931-6111 — Docket Number: GNC26PA

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

GLOBAL NETWORK COMPUTERS

This application is based on and derives priority from U.S. Provisional Application Nos. 60/322,474, filed September 17, 2001, and 60/323,701, filed September 21, 2001, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention relates generally to one or more computer networks that include computers, such as personal computers (PC's) or network computers such as servers, which have microprocessors linked by broadband transmission means and have hardware, software, firmware, and other means such that at least two parallel processing operations occur that involve at least two sets of computers in the network or in interconnected networks. This invention constitutes a form of metacomputing.

More particularly, this invention relates to one or more large networks, like the Internet, which comprise smaller networks and large numbers of interconnected computers, wherein multiple separate parallel or massively parallel processing operations involving multiple different sets of computers occur simultaneously. Even more particularly, this invention relates to one or more such networks wherein multiple parallel or massively parallel microprocessing processing operations occur separately or in an interrelated fashion, and wherein ongoing network processing linkages are established between virtually any microprocessors of separate computers connected to the network.

Still more particularly, this invention relates generally to a network structure or architecture that enables the shared use of network microprocessors for parallel processing, including massive parallel processing, and other shared processing such as multitasking, wherein personal computer owners provide microprocessor processing power to a network, such as for parallel or massively parallel processing or multitasking, in exchange for network linkage to other personal computers and other computers supplied by network providers such as Internet Service Providers (ISP's), including linkage to other microprocessors for parallel or other processing such as multitasking. The financial basis of the shared use between owners and providers may be whatever terms to which the parties agree, subject to governing laws,

regulations, or rules, including payment from either party to the other based on periodic measurement of net use or provision of processing power like a deregulated electrical power grid or involving no payment. The network system may provide an essentially equivalent usage of computing resources by both users and providers since any network computer operated by either entity is potentially both a user and provider of computing resources alternately or simultaneously, assuming multitasking is operative. A user may have an override option exercised on the basis of, for example, a user profile, a user's credit line, or relatively instant payment.

This invention also relates to a network system architecture including hardware and software that provides use of the Internet or other network, without cost, to users of personal computers or other computers, while also providing users with computer processing performance that at least doubles every 18 months through metacomputing means. This metacomputing performance increase provided by the new Grid (or MetaInternet) is in addition to other performance increases, such as those already anticipated by Moore's Law.

The computer industry has been governed over the last 30 years by Moore's Law, which holds that the circuitry of computer chips shrinks substantially each year, yielding a new generation of chips every 18 months with twice as many transistors, such that microprocessor computing power effectively doubles every year-and-a-half.

The long-term trend in computer chip miniaturization is projected to continue unabated over the next few decades. For example, slightly more than a decade ago a 16 kilobit DRAM (dynamic random access memory) memory chip (storing 16,000 data bits) was typical; the standard in 1996 was the 16 megabit chip (16,000,000 data bits), which was introduced in 1993; industry projections are for 16 gigabit memory chips (16,000,000,000 data bits) to be introduced in 2008 and 64 gigabit chips in 2011; and 16 terabit chips (16,000,000,000,000 data bits) may be conceivable by the mid-to-late 2020's, by which time such microchips may have become nanochips in terms of their circuit dimensions. This is a thousand-fold increase regularly every fifteen years. Hard drive speed and capacity are also growing at a spectacular rate, even higher in recent years than that of semiconductor microchips.

Similarly, regular and enormous improvements may continue in microprocessor computing speeds, whether measured in simple clock speed or MIPS (millions of instructions per second) or numbers of transistors per chip. For example, performance has improved by four or five times every three years since Intel launched its X86 family of microprocessors used in the currently dominant "Wintel" standard personal computers. The initial Intel Pentium Pro microprocessor was introduced in 1995 and is a thousand times faster than the first IBM standard PC microprocessor, the Intel 8088, which was introduced in 1979. By 1996 the fastest of microprocessors, such as Digital Equipment Corporation's Alpha chip, and even the microprocessor of the Nintendo 64 video game system, were faster than the processor in the original Cray Y-MP supercomputer.

Microprocessors, software, firmware, and other components are also evolving from 8-bit and 16-bit systems into the 32-bit systems that are becoming the standard today, with some 64-bit systems like the DEC Alpha already introduced and more coming, such as Intel's Itanium microprocessor in 2001, with future increases to 128-bit systems likely.

A second major development trend in the past decade or so has been the rise of parallel processing, a computer architecture utilizing more than one CPU microprocessor linked together into a single computer with new operating systems having modifications that allow such an approach. Thousands of relatively simple microprocessors may be used together for massively parallel processing. The field of supercomputing has been overtaken by this approach, which includes designs utilizing many identical standard personal computer microprocessors.

Hardware, firmware, software, and other components specific to parallel processing are in a relatively early stage of development compared to that for single processor computing. Therefore, much further design and development are expected in the future to better maximize the computing capacity made possible by parallel processing. Continued improvement is anticipated in system hardware, software, and architectures for parallel processing so that reliance on the need for multiple microprocessors to share a common central memory is reduced, thereby allowing more independent operation of those general purpose microprocessors, each with their

own discrete memory, like current personal computers, workstations, and most other computer systems architecture. For unconstrained operation, each individual microprocessor should have rapid access to sufficient memory.

Several models of personal computers having more than one general purpose microprocessor are now available. In the future, personal computers, broadly defined to include versions not currently in use, will likely also employ parallel computing utilizing multiple microprocessors or massively parallel computing with very large numbers of microprocessors. Future designs, such as Intel's Itanium chip, are expected to have a significant number of parallel processors on a single microprocessor chip.

A form of parallel processing called superscalar processing is also being employed within microprocessor design. The current generation of microprocessors, such as the Intel Pentium, have more than one data path within the microprocessor in which data is processed, with two to three paths being typical now and as many as eight in 1998 in IBM's new Power 3 microprocessor chip.

A third major development trend is the increasing size of bandwidth, which is a measure of communications power or transmission speed, in terms of units of data per second, between computers connected by a network. Previously, the local area networks and telephone lines typically linking computers including personal computers have operated at speeds much lower than the processing speeds of a personal computer. For example, a typical 1997 Intel Pentium operates at 100 MIPS, whereas the most common current Ethernet connecting PC's is roughly 10 times slower at 10 megabits per second (Mbps), although some Ethernet connections are now 100 Mbps and telephone lines are very much slower, the highest typical speed in 1998 being the approximately 56 kilobits reachedduring downloads.

The situation is expected to change dramatically. Bandwidth or transmission speed is anticipated to expand from 5 to 100 times as fast as the rise of microprocessor speeds, due to the use of coaxial cable, wireless, and especially fiber optic cable and optical wireless, instead of old telephone twisted pair lines, and due to the use of wideband communication such as dense wave division multiplexing (DWDM) and wideband code division multiple access (CDMA), as well as

ultrawideband wireless. In DWDM systems, multiple channels are transmitted over a single fiber because they are sent at different wavelengths. Telecommunication providers are now making available single fiber connections supporting a bandwidth of 40 gigabits per single fiber, and, alternatively, as many as 160 wavelength channels (lambdas) per single fiber. In CDMA systems, users are multiplexed across the same spectrum, with each user being assigned a different instance of a noise-like carrier wave.

Technical improvements are expected in the near term which will make it possible to carry over 2 gigahertz (billions of cycles per second) on each of 700 wavelength channels (lambdas), adding up to more than 1,400 gigahertz on a single fiber thread. Experts have estimated that the bandwidth of optical fiber has been utilized one million times less fully than the bandwidth of coaxial or twisted pair copper lines. Within a decade, 10,000 wavelength streams per fiber are expected; 20 to 80 wavelengths on a single fiber is already commercially available. The use of thin mirrored hollow wires or tubes called omniguides may also provide very substantial additional increases.

Other network connection developments, such as asynchronous transfer mode (ATM) and digital signal processors, whose price/performance ratio has improved tenfold every two years, are also supporting the rapid increase in bandwidth. The increase in bandwidth reduces the need for switching, and switching speed will be greatly enhanced when practical optical switches are introduced in the near future, potentially reducing costs substantially.

The result of this huge bandwidth increase is extraordinary: already it is technically possible to connect virtually any computer to a network with a bandwidth that equals or exceeds the computer's own internal system bus speed, even as that bus speed itself is increasing significantly. The principal constraint is the infrastructure, consisting mostly of connecting the "last mile" to personal computers with optical fiber or other broad bandwidth connections, which still need to be built. The system bus of a computer is its internal network connecting many or most of its internal components such as microprocessor, random access memory (RAM), hard drive, modem, floppy drive, and CD-ROM; for recent personal computers, the system bus

has been only about 40 megabits per second, but is up to 133 megabits per second on Intel's Pentium PCI bus in 1995. IBM's 1998 Power3 microprocessor chip has a system bus of 1.6 gigabits per second and there is now up to a gigabit per second on Intel's Pentium PCI bus.

Despite these tremendous improvements anticipated in the future, a typical PC is already so fast that its microprocessor is essentially idle during most of the time the PC is in actual use, and the operating time itself is but a small fraction of those days the PC is even in use at all. Nearly all PC's are essentially idle during roughly all of their useful life. A microprocessor of a PC may be in an idle state 99.9% of the time, disregarding unnecessary microprocessor busywork such as executing screen saver programs, which have been made essentially obsolete by power-saving CRT monitor technology, which is now standard in the PC industry.

Because the reliability of PC's is so exceptionally high now, with the mean time to failure of all components typically several hundred thousand hours or more, the huge idle time of PC's represents a total loss; given the high capital and operating costs of PC's, the economic loss is very high. PC idle time does not in effect store a PC, saving it for future use, since the principle limiting factor to continued use of today's PC's is obsolescence, not equipment failure resulting from use.

Moreover, there is continuing concern that Moore's Law, which holds that the constant miniaturization of circuits results in a doubling of computing power every 18 months, cannot continue to hold true much longer. Indeed, Moore's Law may now be nearing its limits for silicon-based devices, perhaps by as early as 2010. No new technologies have yet emerged that seem to have the potential for development to a practical level by then, although many recent advances have the potential to maintain Moore's Law.

SUMMARY OF THE INVENTION

However, the confluence of all three of the established major trends summarized above--supercomputer-like personal computers, the spread of parallel processing using personal computer general purpose microprocessors (particularly massively parallel processing), and the enormous increase in network

communications bandwidth--enables a solution to the excessive idleness problem of personal computers and the possible end of Moore's Law. The solution may achieve very high potential economic savings once the basic infrastructure connecting personal computers with optical fiber is in place in the relatively near future.

The solution is to use those mostly idle PC's (or their equivalents or successors) to build a parallel or massively parallel processing computer or computers utilizing a very large network, like the Internet or, more specifically, like the World Wide Web (WWW), or their equivalents or eventual successors like the Grid or MetaInternet (and including Internet II and the Next Generation Internet, which are under development now and which will utilize much broader bandwidth and will coexist with the Internet, the structure of which is in ever constant hardware and software upgrade and including the SuperInternet based on essentially all optical fiber transmission) with extremely broad bandwidth connections and virtually unlimited data transmission speed.

A prime characteristic of the Internet is the very large number of computers of all sorts already linked thereto, with the future potential for an effectively universal connection. The Internet is a network of networks of computers that provides nearly unrestricted access worldwide. The currently existing and soon-to-be widely available very broad bandwidth of network communications is used to link personal computers externally in a manner at least equivalent to, and probably much faster than, the faster internal system buses of the personal computers, so that no external processing constraint is imposed on linked personal computers by data input, output, or throughput; the speed of the microprocessor itself and the internal connections or buses of the PC are the only processing constraint of the system.

This makes possible efficient external parallel processing (and multitasking), including massively parallel processing, in a manner paralleling more conventional internal parallel processing, called superscalar processing.

In one embodiment, the World Wide Web is transformed into a huge virtual massively parallel processing computer or computers, with potential through its established hyperlinks connections to operate in a manner at least somewhat like a neural network or neural networks, since the speed of transmission in the broadband

linkages is so great that any linkage between two microprocessors is virtually equivalent to direct, physically close connections between those microprocessors.

With further development, digital signal processor-type microprocessors and/or analogue microprocessors may be particularly advantageous for this approach, either alone or in conjunction with conventional microprocessors and/or the new microprocessors described below. Networks with WWW-type hyperlinks incorporating digital signal processor-type microprocessors could operate separately from networks of conventional microprocessors or with one or more connections between such differing networks or with relatively complete integration between such differing networks. Simultaneous operation across the same network connection structure should be possible, employing non-interfering transmission links.

Such extremely broad bandwidth networks of computers enable every PC within the network to be fully utilized or nearly so. Because of the extraordinary extent to which existing PC's are currently idle, at optimal performance this new system may result in a thousand-fold increase in computer power available to each and every PC user, and, on demand, almost any desired level of increased power, limited mostly by increased cost, which however are relatively far less than possible from other conceivable computer network configurations. This revolutionary increase is in addition to the extremely rapid, but evolutionary increases already occurring in the computer/network industry, as discussed above.

The metacomputing hardware and software means of the Grid (or MetaInternet) provides performance increases that are likely to at least double every eighteen months based on the doubling of personal computers shared in a typical parallel processing operation by a standard PC user, starting first with at least 2 PC's, then about 4, about 8, about 16, about 32, about 64, about 128, about 256, and about 512, for example. After about fifteen years, for example, it is anticipated that each standard PC user will likely be able to use a maximum of about 1,024 personal computers for parallel processing or any other shared computing use, while generally using for free the Internet or its successors, like the Grid (or MetaInternet). At the other end of the performance spectrum, supercomputers experience a similar performance increase generally, but ultimately the performance increase is limited

primarily by the cost of adding network linkages to available PC's, so there is definite potential for a huge leap in supercomputer performance.

Network computer systems as described above offer almost limitless flexibility due to the abundant supply of heretofore idle connected microprocessors. This advantage allows "tightly coupled" computing problems, which normally are difficult to process in parallel, to be solved without knowing in advance how many processors are available (as is now necessary in relatively massively parallel processing), what they are, and their connection characteristics. A minimum number of equivalent processors (with equivalent other specifications) are easily found nearby in a massive network like the Internet and assigned within the network from those multitudes available nearby. Moreover, the number of microprocessors used are almost completely flexible, depending on the complexity of the problem, and limited only by cost. The existing problem of time delay is solved largely by the widespread introduction of broad bandwidth connections between computers processing in parallel.

The state of the known art relating to this application is summarized in The Grid: Blueprint for a New Computing Infrastructure, edited by Ian Foster and Carl Kesselman, and published by Morgan Kaufman Publishers, Inc. in 1998. The state of the known art relating to this application is also summarized in: Scalable Parallel Computing by Kai Hwang and Zhiwei Xu, published by WCB McGraw-Hill in 1998; Parallel Programming by Barry Wilkinson and Michael Allen, published by Prentice Hall in 1998; Computer Architecture: A Quantitative Approach (2nd Edition) by David Patterson and John Hennessy, published by Morgan Kaufmann in 1996; Parallel Computer Architecture by David Culler and Jaswinder Singh, published by Morgan Kaufman in 1998; and Computer Organization and Design by John Hennessy and David Patterson, published by Morgan Kaufman in 1998.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a meter means which measures flow of

computing during a shared operation such as parallel processing between a typical PC user and a network provider.

Figure 2 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of another meter means which measures the flow of network resources, including shared processing, being provided to a typical PC user and a network provider.

Figure 3 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of another meter means which, prior to execution, estimates the level of network resources, and their cost, of a shared processing operation requested by a typical PC user from a network provider.

Figures 4A-4C are simplified diagrams of a section of a computer network, such as the Internet, showing in a sequence of steps an embodiment of a selection means whereby a shared processing request by a PC is matched with a standard preset number of other PC's to execute a shared operation.

Figures 5A and 5B are simplified diagrams of a section of a computer network, such as the Internet, showing embodiments of a control means whereby the PC, when idled by its user, is made available to the network for shared processing operations.

Figure 6 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a signal means whereby the PC, when idled by its user, signals its availability to the network for shared processing operations.

Figure 7 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a receiver and/or interrogator means whereby the network receives and/or queries the availability for shared processing status of a PC within the network.

Figure 8 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a selection and/or utilization means whereby the network locates available PC's in the network that are located closest to each other for shared processing.

Figure 9 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a system architecture for conducting a

request imitated by a PC for a search using parallel processing means that utilizes a number of networked PC's.

Figures 10A-10I are simplified diagrams of a section of a computer network, such as the Internet, showing an embodiment of a system architecture utilizing an internal firewall to separate that part of a networked PC (including a system reduced in size to a microchip) that is accessible to the network for shared processing from a part that is kept accessible only to the PC user; also showing the alternating role that each PC in the network may play as either a master or slave in a shared processing operation involving one or more slave PC's in the network; and showing a home or business network system which can be configured as an Intranet; in addition, showing PC and PC microchips controlled by a controller (including remote) with limited or no processing capability; and showing PC and PC microchips in which an internal firewall 50 can be reconfigured by a PC user.

Figure 11 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a system architecture for connecting clusters of PC's to each other by wireless means, to create the closest possible (and therefore fastest) connections.

Figure 12 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a system architecture for connecting PC's to a satellite by wireless means.

Figure 13 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a system architecture providing a cluster of networked PC's with complete interconnectivity by wireless means.

Figure 14A is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a transponder means whereby a PC can identify one or more of the closest available PC's in a network cluster to designate for shared processing by wireless means. Figure 14B shows clusters connected wirelessly. Figure 14C shows a wireless cluster with transponders and with a network wired connection to the Internet. Figure 14D shows a network client/server wired system with transponders.

Figure 15 is a simplified diagram of a section of a computer network, such as the Internet, showing an embodiment of a routing means whereby a PC request for shared processing is routed within a network using broad bandwidth connection means to another area in a network with one or more idle PC's available.

Figures 16A-16Z, 16AA, and 16AB show a new hierarchical network architecture for personal computers and/or microprocessors based on subdivision of parallel processing or multi-tasking operations through a number of levels down to a processing level.

Figures 17A-17D show an internal firewall 50 with a dual function, including that of protecting Internet users (and/or other network users sharing use) of one or more slave personal computers PC 1 or microprocessors 40 from unauthorized surveillance or intervention by an owner/operator of those slave processors.

Figures 18A-18D show designs for one or more virtual quantum computers integrated into one or more digital computers.

Figure 19 shows special adaptations to allow the use of idle automobile computers to be powered and connected to the Internet (or other net) for parallel or multi-tasking processing.

Figures 20A and 20B show separate broad bandwidth outputs or inputs such as an optical connection like glass fiber from each microprocessor 40 or 94.

Figures 21A and 21B are similar to Figures 20A and 20B, but show additionally that all microprocessors of a personal computer or personal computer on a microchip can have a separate input/output communication link to a digital signal processor (DSP) or other transmission/reception connection component. Figure 21C shows a H-tree configuration of binary tree networks.

Figure 22A shows a PC microprocessor on a microchip similar to that of Figure 21B, except that Figure 22A shows microprocessors 93 and 94 each connecting to an optical wired connection 99' such as thin mirrored hollow wire or optical omniguide or optical fiber.

Figures 23A-23E show multiple firewalls 50 within a personal computer 1 or PC microchip 90.

Figure 24 shows a hard drive with an internal firewall 50.

Figures 25A-25D show the use for security of power interruption or data overwrite of volatile memory like DRAM and non-volatile memory like Flash or MRAM (or ovonics), respectively, of the network portion of a personal computer PC1 or system on a microchip PC90.

Figures 26A-26C show exemplary microchip and photovoltaic cell embodiments.

Figures 27A-27H show exemplary microchip and Faraday Cage embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments useful for a network of computers are presented. In an embodiment, an apparatus includes a microchip and a Faraday Cage. The microchip includes a personal computer with a general purpose microprocessor on the microchip. The Faraday Cage surrounds at least a portion of the microchip. In another embodiment, an apparatus includes a microchip. The microchip includes a general purpose microprocessor and one or more photovoltaic cells.

The new network computer utilizes PC's as providers of computing power to the network, not just users of network services. These connections between network and personal computer are enabled by a new form of computer/network financial structure that is rooted in the fact that economic resources being provided the network by PC owners (or leaser) are similar in value to those being provided by the network provider providing connectivity.

Unlike existing one-way functional relationships between PC users and network providers such as internet service providers, which often currently utilize telecommunications networks for connectivity, wherein the network provider provides access to a network like the Internet for a fee, much like cable TV services, this new relationship recognizes that the PC user is also providing the network access to the user's PC for parallel computing use, which has a similar value. The PC thus both provides and uses services on the network, alternatively or potentially even virtually simultaneously, in a multitasking mode.

This new network operates with a structural relationship that is roughly like that which presently exists between an electrical power utility and a small

independent power generator connected to a deregulated utility's electrical power grid, wherein electrical power can flow in either direction between utility and independent generator depending on the operating decisions of both parties, and at any particular point in time each party is in either a debt or credit position relative to the other based on the net direction of that flow for a given period, and each party is billed accordingly. In the increasingly deregulated electrical power industry, electrical power, in terms of creation and transmission, is becoming a commodity bought and sold in a competitive marketplace that crosses traditional borders. With the structural relationship proposed herein for the new network, parallel free market structures can develop over time in a new computer power industry dominated by networks of personal computers in all their forms providing shared processing in a grid scaling almost seamlessly from local to national to international like an open market electrical power grid.

For this new network and its structural relationships, a network provider or Internet service provider (ISP) is defined in the broadest possible way as any entity (corporation or other business, government, not-for-profit, cooperative, consortium, committee, association, community, or other organization or individual) that provides personal computer users (very broadly defined below) with initial and continuing connection hardware and/or software and/or firmware and/or other components and/or services to any network, such as the Internet and WWW or Internet II or Next Generation Internet (NGI) or their present or future equivalents, coexistors, or successors, like the herein proposed Grid (or MetaInternet), including any of the current or future types of Internet access providers (ISP's) including telecommunication companies, television cable or broadcast companies, electrical power utilities or other related companies, satellite communications companies, or their present or future equivalents, coexistors or successors.

The connection means used in the networks of the network providers, including between personal computers or equivalents or successors, may be very broad bandwidth, including electromagnetic connections and optical connections, including wired like fiber optic cable or wireless like optical wireless, for example, but not excluding any other electromagnetic or other means, including television

coaxial cable and telephone twisted pair, as well as associated gateways, bridges, routers, and switches with all associated hardware and/or software and/or firmware and/or other components and their present or future equivalents or successors. The computers used by the Internet service providers include any current or future computers, including such current examples as mainframes, minicomputers, servers, and personal computers, and their associated hardware and/or software and/or firmware and/or other components, and their present or future equivalents or successors.

Other levels of network control beyond the Internet or other network service provider also exist to control any aspect of the parallel processing network structure and function, any one of which levels may or may not control and interact directly with the PC user. For example, at least one level of network control like the World Wide Web Consortium (W3C) or Internet Society (ISOC) or other ad hoc industry consortia establish and ensure compliance with any prescribed parallel processing network standards and/or protocols and/or industry standard agreements for any hardware and/or software and/or firmware and/or other component connected to the network. Under the consensus control of these consortia/societies, other levels of the parallel processing network control can deal with administration and operation of the network. These other levels of the parallel processing network control can potentially be constituted by any network entity, including those defined immediately above for network providers.

The principal defining characteristic of the parallel processing network herein described is communication connections (including hardware and/or software and/or firmware and/or other component) of any form, including electromagnetic (such as radio or microwaves and including light) and electrochemical (and not excluding biochemical or biological), between PC users and their computers, with connection (either directly or indirectly) to the largest number possible of users and their computers and microprocessors being highly advantageous, such as networks like the Internet (and Internet II and the Next Generation Internet) and WWW and equivalents and successors, like the Grid (or MetaInternet). Multiple levels of such networks will likely coexist with different technical capabilities, like Internet and Internet II, but

have interconnection and therefore communicate freely between levels, for such standard network functions as electronic mail, for example.

A personal computer (PC) user is defined in the broadest possible way as any individual or other entity routinely using a personal computer, which is defined as any computer, such as digital or analog or neural or quantum, particularly including personal use microprocessor-based personal computers having one or more general purpose microprocessors (each including one or more parallel processors) in their general current form, including hardware with fixed or reconfigurable circuitry (such as field-programmable gate array or FPGA) and/or electro-mechanical components (including micro or nano sized) and/or optical components, including all-optical, and/or software and/or firmware and/or any other component and their present and future equivalents or successors, such as application-specific (or several application) computers, network computers, handheld personal digital assistants, personal communicators such as telephones and pagers, wearable computers, digital signal processors, neural-based computers (including PC's), entertainment devices such as televisions and associated cable digital set-top control boxes, video tape recorders, video electronic games, videocams, compact or digital video disk (CD or DVD) player/recorders, radios and cameras, other household electronic devices, business electronic devices such as printers, copiers, fax machines, footwear, automobile or other transportation equipment devices, robots, toys, and other electronic devices, especially including those owned (or leased directly or indirectly) and used directly by individuals, utilizing one or more microprocessors, including those made of inorganic compounds such as silicon and/or other inorganic or organic (including biological, such as DNA) compounds, and other current or successor devices incorporating one or more microprocessors (or functional or structural equivalents), including routers, switches, and other network devices,as well as current and future forms of mainframe computers, minicomputers, workstations, and even supercomputers, as well as routers, switches, and other electrical or optical network devices (or microelectro-mechanical devices such as MEMS), that can be considered as PCs in the distributed processing network described herein, since they can be used functionally in the same general way in the network as a PC or a PC can be used to perform their functions, at least in a

limited fashion alone or more effectively in numbers that are aggregated together or distributed. Such personal computers as defined above have owners or leasers, which may or may not be the same as the computer users. Continuous connection of computers to the network, such as the Internet, WWW, or equivalents or successors, is not required, since connection can also be made at the initiation of a shared processing operation.

Parallel processing is defined as one form of shared processing involving two or more microprocessors used in solving the same computational problem or other task. Massively parallel microprocessor processing involves large numbers of microprocessors. In today's technology, massive parallel processing is probably to be considered to be about 64 microprocessors (referred to in this context as nodes) and over 7,000 nodes have been successfully tested in an Intel supercomputer design using PC microprocessors (Pentium Pros). It is anticipated that continued software improvements will make possible effective use of a much larger number of nodes, very possibly limited only by the number of microprocessors available for use on a given network, even an extraordinarily large one like the Internet or its equivalents and/or successors, like the Grid (or MetaInternet). Shared processing also includes multitasking, which is unrelated processing in parallel.

Broadband wavelength or broad bandwidth network transmission is defined here to mean a transmission speed (usually measured in bits per second) that is at least high enough (or roughly at least equivalent to the internal clock speed of the microprocessor or microprocessors times the number of microprocessor channels equaling instructions per second or operations per second or calculations per second) so that the processing input and output of the microprocessor is substantially unrestricted, particularly including at peak processing levels, by the bandwidth of the network connections between microprocessors that are performing some form of parallel processing, particularly including massive parallel processing. Since this definition is dependent on microprocessor speed, it increases as microprocessor speeds increase. For microchips with more than one processor, the network connection to the microchip may have bandwidth broad enough to ensure that all of

the microprocessors are unrestricted by a bottleneck at the connection during the microprocessors' peak processing levels.

However, a connection means referenced above is a light wave or optical waveguide connection such as fiber optic cable, which in 1996 already provided multiple gigabit bandwidth on single fiber thread and is rapidly improving significantly on a continuing basis, so the general use of optical waveguide connections such as fiber between PCs may assure broad bandwidth for data transmission that is far greater than microprocessor and associated internal bus speed to provide data to be transmitted. In addition, new wired optical connections or waveguide in the form of thin, mirrored hollow wires or tubes called omniguides offer even much greater bandwidth than optical fiber and without need for amplification when transmitting over distances, unlike optical fiber. The connection means to provide broad bandwidth transmission is either wired or wireless, with wireless (especially optical) generally provided for mobile personal computers (or equivalents or successors) and as otherwise indicated below. Wireless connection bandwidth is also increasing rapidly and optical wireless bandwidth is considered to offer essentially the same benefit as fiber optic cable: data transmission speed that exceeds data processing speed.

The financial basis of the shared use between owners/ leasers and providers is whatever terms to which the parties agree, subject to governing laws, regulations, or rules, including payment from either party to the other based on periodic measurement of net use or provision of processing power, in a manner like an deregulated or open market electrical power grid.

In one embodiment, as shown in Figure 1, in order for this network structure to function effectively, there is a meter device 5 (comprising hardware and/or software and/or firmware and/or other component) to measure the flow of computing power between PC 1 user and network 2 provider, which may provide connection to the Internet and/or World Wide Web and/or Internet II and/or any present or future equivalent or successor 3, like the Grid (or MetaInternet). In one embodiment, the PC user may be measured by some net rating of the processing power being made available to the network, such as net score on one or more standard tests measuring

speed or other performance characteristics of the overall system speed, such as PC Magazine's benchmark test program, ZD Winstone (potentially including hardware and/or software and/or firmware and/or other component testing) or specific individual scores for particularly important components like the microprocessor (such as MIPS or millions of instructions per second) that may be of application-specific importance, and by the elapsed time such resources were used by the network. In the simplest case, for example, such a meter need measure only the time the PC was made available to the network for processing 4, which can be used to compare with time the PC used the network (which is already normally measured by the provider, as discussed below) to arrive at a net cost; potential locations of such a meter include at a network computer such as a server, at the PC, and at some point on the connection between the two. Throughput of data in any standard terms is another potential measure.

In another embodiment, as shown in Figure 2, there also is a meter device 7 (comprised of hardware and/or software and/or firmware and/or other component) that measures the amount of network resources 6 that are being used by each individual PC 1 user and their associated cost. This includes, for example, time spent doing conventional downloading of data from sites in the network or broadcast from the network 6. Such metering devices currently exist to support billing by the hour of service or type of service, as is common in the public industry, by providers such as America Online, Compuserve, and Prodigy. The capability of such existing devices is enhanced to include a measure of parallel processing resources that are allocated by the Internet Service Provider or equivalent to an individual PC user from other PC users 6, also measured simply in time. The net difference in time 4 between the results of meter 5 and meter 7 for a given period provides a reasonable billing basis.

Alternately, as shown in Figure 3, a meter 10 also estimates to the individual PC user prospectively the amount of network resources needed to fulfill a processing request from the PC user to the network (provider or other level of network control) and associated projected cost, provides a means of approving the estimate by executing the request, and a realtime readout of the cost as it occurs (alternatively, this meter may be done only to alert 9 the PC user that a given processing request 8 falls

outside normal, previously accepted parameters, such as level of cost). For an unusually deep search request, a priority or time limit and depth of search may be criteria or limiting parameters that the user can determine or set with the device, or that can be preset, for example, by the network operating system of the ISP or by the operating system of the PC or other components of the parallel processing system.

The network may involve no payment between users and providers, with the network system (software, hardware, etc.) providing an essentially equivalent usage of computing resources by both users and providers (since any network computer operated by either entity can potentially be both a user and provider of computing resources (even simultaneously, assuming multitasking), with potentially an override option by a user (exercised on the basis, for example, of user profile or user's credit line or through relatively instant payment).

As shown in Figures 4A-4C, the priority and extent of use of PC and other users may be controlled on a default-to-standard-of-class-usage basis by the network (provider or other) and overridden by the user decision on a basis prescribed by the specific network provider (or by another level of network control). One example of a default basis is to expend up to a PC's or other user's total credit balance with the provider described above and the network provider then to provide further prescribed service on a debt basis up to some set limit for the user; different users may have different limits based on resources and/or credit history.

A specific category of PC user based, for example, on specific microprocessor hardware owned or leased, may have access to a set maximum number of parallel PC's or microprocessors, with smaller or basic users generally having less access and vice versa. Specific categories of users may also have different priorities for the execution of their processing by the network other than the simplest case of first come, first served (until complete). A very wide range of specific structural forms between user and provider are possible, both conventional and new, based on unique features of the new network computer system of shared processing resources.

For example, in the simplest case, in an initial system embodiment, as shown in Figure 4A, a standard PC 1 user request 11 for a use involving parallel processing may be defaulted by system software 13, as shown in Figure 4B, to the use of only

one other essentially identical PC 1_2 microprocessor for parallel processing or multitasking, as shown in Figure 4C; larger standard numbers of PC microprocessors, such as about three PC's at the next level, as shown in later Figure 10G (which could also illustrate a PC 1 user exercising an override option to use a level of services above the default standard of one PC microprocessor, presumably at extra cost), for a total of about four, then about 8, about 16, about 32, about 64, and so on, or virtually any number in between, is made available as the network system is upgraded in simple phases over time, as well as the addition of sophisticated override options. As the phase-in process continues, many more PC microprocessors can be made available to the standard PC user (virtually any number), starting at about 128, for example, then about 256, then about 512, then about 1024 and so on over time, as the network and all of its components are gradually upgraded to handle the increasing numbers. System scalability at even the standard user level is essentially unlimited over time.

For most standard PC users (including present and future equivalents and successors), connection to the Internet or present or future equivalents or successors like the Grid (or MetaInternet) may be at no cost to PC users, since in exchange for such Internet access the PC users can generally make their PC, when idle, available to the network for shared processing. Competition between Internet Service Providers (including present and future equivalents and successors) for PC user customers may be over such factors as the convenience and quality of the access service provided and of shared processing provided at no additional cost to standard PC users, or on such factors as the level of shared processing in terms, for example, of number of slave PC's assigned on a standard basis to a master PC. The ISP's can also compete for parallel processing operations, from inside or outside the ISP Networks, to conduct over their networks.

In addition, as shown in Figures 5A-5B, in another embodiment there is a (hardware and/or software and/or firmware and/or other) controlling device to control access to the user's PC by the network. In its simplest form, such as a manually activated electromechanical switch, the PC user could set this controller device to make the PC available to the network when not in use by the PC user. Alternatively, the PC user could set the controller device to make the PC available to the network

whenever in an idle state, however momentary, by making use of multitasking hardware and/or software and/or firmware and/or other component (broadcast or "push" applications from the Internet or other network could still run in the desktop background).

Or, more simply, as shown in Figure 5A, whenever the state that all user applications are closed and the PC 1 is available to the network 14 (perhaps after a time delay set by the user, like that conventionally used on screensaver software) is detected by a software controller device 12 installed in the PC, the device 12 signals 15 the network computer such as a server 2 that the PC available to the network, which could then control the PC 1 for parallel processing or multitasking by another PC. Such shared processing can continue until the device 12 detects an application being opened 16 in the first PC (or at first use of keyboard, for quicker response, in a multitasking environment), when the device 12 signals 17 the network computer such as a server 2 that the PC is no longer available to the network, as shown in Figure 5B, so the network can then terminate its use of the first PC.

In the embodiment shown in Figure 6, there is a (hardware and/or software and/or firmware and/or other component) signaling device 18 for the PC 1 to indicate or signal 15 to the network the user PC's availability 14 for network use (and whether full use or multitasking only) as well as its specific (hardware/software/firmware/other components) configuration 20 (from a status 19 provided by the PC) in sufficient detail for the network or network computer such as a server 2 to utilize its capability effectively. In one embodiment, the transponder device is resident in the user PC and broadcasts its idle state or other status (upon change or periodically, for example) or responds to a query signal from a network device.

Also, in another embodiment, as shown in Figure 7, there is a (hardware/software and/or firmware and/or other component) transponder device 21 resident in a part of the network (such as network computer, switch, router, or another PC, for example) that receives 22 the PC device status broadcast and/or queries 26 the PC for its status, as shown in Figure 7.

In one embodiment, as shown in Figure 8, the network grid also has resident in a part of its hardware and/or software (and/or firmware and/or other components) a capacity such as to allow it to most effectively select and utilize the available user PC's to perform parallel processing initiated by PC users or the network providers or others. To do so, the network grid should have the (hardware and/or software and/or firmware and/or other component) capability of locating each PC accurately at the PC's position on the geographic grid lines/connection means 23 so that parallel processing occurs between PC's (PC 1 and PC 1_2) as close together as possible, which should not be difficult for PC's at fixed sites with a geographic location, customarily grouped together into cells 24, as shown in Figure 8, but which requires an active system for any wireless microprocessor to measure its distance from its network relay site, as discussed below in Figure 14.

One of the primary capabilities of the Internet (or Internet II or successor, like the Grid or MetaInternet) or WWW network computer is to facilitate searches by the PC user or other user. As shown in Figure 9, searches are particularly suitable to multiple processing, since, for example, a typical search is to find a specific Internet or WWW site with specific information. Such site searches can be broken up geographically, with a different PC processor 1' allocated by the network communicating through a wired means 99 as shown (or wireless connections) to search each area, the overall area being divided into eight separate parts, as shown, which may be about equal, so that the total search would be about 1/8 as long as if one processor did it alone (assuming the PC 1 microprocessor provides control only and not parallel processing).

As a typical example, a single PC user might need 1,000 minutes of search time to find what is requested, whereas the network computer, using multiple PC processors, might be able to complete the search in 100 minutes using 10 processors, or 10 minutes using 100 processors or 1 minute using 1,000 processors (or even 1 second using 60,000 processors), assuming performance transparency, which should be achievable, at least over time, even for massive numbers of parallel processors. The parallel processing network's external parallel processing may be completely scalable, with virtually no theoretical limit.

The above examples also illustrates a tremendous potential benefit of network parallel processing. The same amount of network resources, 60,000 processor seconds, was expended in each of the equivalent examples. But by using relatively large multiples of processors, the network can provide the user with relatively immediate response with no difference in cost (or relatively little difference) -- a major benefit. In effect, each PC user linked to the network providing external parallel processing becomes, in effect, a virtual supercomputer. As discussed below, supercomputers can experience a similar spectacular leap in performance by employing a thousand-fold (or more) increase in microprocessors above current levels.

Such power will likely be required for any effective searches in the World Wide Web (WWW). WWW is currently growing at a rate such that it is doubling every year, so that searching for information within the WWW will become geometrically more difficult in future years, particularly a decade hence, and it is already a very significant difficulty to find WWW sites of relevance to any given search and then to review and analyze the contents of the site.

In addition, many more large databases are being made Web accessible and the use of Extensible Markup Language (XML) will accelerate that trend. Moreover, existing search engine results list information from a prior general search and merely summarized on the web servers of search engine operators, whereas embodiments of the present invention allow a further contemporaneous specifically targeted search directed by the PC user utilizing search engine results only as a starting point for much greater depth and analysis allowed by the shared use of many other PC's in a parallel processing operation.

Therefore, the capability to search with massive parallel processing can dramatically enhance the capabilities of scientific, technological and medical researchers.

Such enhanced capabilities for searching (and analysis) can also fundamentally alter the relationship of buyers and sellers of any items and/or services. For the buyer, massive parallel network processing can make it possible to find the best price, worldwide, for any product or the most highly rated product or service (for

performance, reliability, etc.) within a category or the best combination of price/performance or the highest rated product for a given price point and so on. The best price for the product can include best price for shipping within specific delivery time parameters acceptable to the buyer.

For the seller, such parallel processing can drastically enhance the search, worldwide, for customers potentially interested in a given product or service, providing very specific targets for advertisement. Sellers and producers can know their customers directly and interact with them directly for feedback on specific products and services to better assess customer satisfaction and survey for new product development.

Similarly, the vastly increased capability provided by the system's shared parallel processing can produce major improvements in complex simulations like modeling worldwide and local weather systems over time, as well as design and testing of any structure or product, from airliners and skyscrapers to new drugs and to the use of much more sophisticated artificial intelligence (AI) in medical treatment and in sorting through and organizing the PC users' voluminous input of electronic data from "push" technologies. Improvements in games also result, especially in terms of realistic simulation and realtime interactivity.

The Internet or WWW network computer system like the Grid (or MetaInternet) can put into the hands of the PC user an extraordinary new level of computer power vastly greater than the most powerful supercomputer existing today. The world's total of microchips was already about 350 billion in 1997, of which about 15 billion are microprocessors of some kind; most are fairly simple "appliance" type microchips running wrist watches, televisions, cameras, cars, telephones, etc. Assuming growth at its current rates, in a decade the Internet/Internet II/WWW may have a billion individual PC users, each providing an average total of at least 10 highly sophisticated microprocessors (assuming PC's with at least 4 microprocessors (or more, such as 16 microprocessors or 32, for example) and associated other handheld, home entertainment, and business devices with microprocessors or digital processing capability, like a digital signal processor or successor devices. That results in a global computer a decade from now made of at least 10 billion microprocessors,

interconnected by broad bandwidth electromagnetic wave means at speeds approaching the speed of light.

In addition, the exceptionally numerous special purpose "appliance" microprocessors noted above, especially those that operate now intermittently like personal computers, may be designed to the same basic consensus industry standard used for parallel microprocessors for PC's (or equivalents or successors) or for PC "systems on a chip", discussed later in Figures 10A-H, so that all PCs and microprocessors function homogeneously or are homogeneous in the parallel processing Internet. If such PCs and appliance microprocessors are also connected by any broad bandwidth means including fiber optic cable or optical wireless or other wireless, then the number of parallel processors potentially available can increase roughly about 10 times, for a net potential "standard" computing performance of up to 10,000 times current performance within fifteen years, exclusive of Moore's Law routine increases. Web-based ubiquitous computing would become a reality, in terms either of direct connection to the Web or use of common Web standards.

Moreover, in an environment where all current intermittently operating microprocessors follow the same basic design standards so that all are homogeneous parallel processors, then although the cost per microprocessor increases somewhat, especially initially, the net cost of computing for all users falls drastically due to the general performance increase due to the use of billions of otherwise idle "appliance" microprocessors. Therefore, the overall system cost reduction compels a transformation of virtually all such microprocessors, which are currently specialty devices known as application-specific integrated circuits (ASICs), into general microprocessors (like PC's), with software and firmware providing most of their distinguishing functionality. As noted above, homogeneity of parallel (and multi-tasking) processing design standards for microprocessors and network, including local and Internet, may be employed, but heterogeneity is also a well established parallel processing alternative providing significant benefits compared to non-parallel processing.

A typical supercomputer today utilizing the latest PC microprocessors has less than a hundred. Using network linkage to all external parallel processing, a peak

maximum of perhaps 1 billion microprocessors can be made available for a network supercomputer user, providing it with the power 10,000,000 times greater than is available using current conventional internal parallel processing supercomputers (assuming the same microprocessor technology). Because of its virtually limitless scalability mentioned above, resources made available by the network to the supercomputer user or PC user can be capable of varying significantly during any computing function, so that peak computing loads can be met with effectively whatever level of resources are necessary.

In summary, regarding monitoring the net provision of power between PC and network, Figures 1-9 show embodiments of a system for a network of computers, including personal computers, comprising: means for network services including browsing functions, as well as shared computer processing such as parallel processing, to be provided to the personal computers within the network; at least two personal computers; means for at least one of the personal computers, when idled by a personal user, to be made available temporarily to provide the shared computer processing services to the network; and means for monitoring on a net basis the provision of the services to each personal computer or to the personal computer user. In addition, Figures 1-9 show embodiments including where the system is scalar in that the system imposes no limit to the number of the personal computers, including at least 1024 personal computers; the system is scalar in that the system imposes no limit to the number of personal computers participating in a single shared computer processing operation, including at least 256 personal computers; the network is connected to the Internet and its equivalents and successors, so that the personal computers include at least a million personal computers; the network is connected to the World Wide Web and its successors; the network includes at least one network server that participates in the shared computer processing; the monitoring means includes a meter device to measure the flow of computing power between the personal computers and the network; the monitoring means includes a means by which the personal user of the personal computer is provided with a prospective estimate of cost for the network to execute an operation requested by the personal user prior to execution of the operation by the network; the system has a control means by

which to permit and to deny access to the personal computers by the network for shared computer processing; access to the personal computers by the network is limited to those times when the personal computers are idle; and the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data transmission that is at least greater than a peak data processing speed of the microprocessor.

Also, relative to maintaining a standard cost, Figures 1-9 show embodiments of a system for a network of computers, including personal computers, comprising: means for network services including browsing functions, as well as shared computer processing such as parallel processing, to be provided to the personal computers within the network; at least two personal computers; means for at least one of the personal computers, when idled by a personal user, to be made available temporarily to provide the shared computer processing services to the network; and means for maintaining a standard cost basis for the provision of the services to each personal computer or to the personal computer user. In addition, Figures 1-9 show embodiments including where the system is scalar in that the system imposes no limit to the number of personal computers, including at least 1,024 personal computers; the system is scalar in that the system imposes no limit to the number of the personal computers participating in a single shared computer processing operation, including at least 256 personal computers; the network is connected to the Internet and its equivalents and successors, so that the personal computers include at least a million personal computers; the standard cost is fixed; the fixed standard cost is zero; the means for maintaining a standard cost basis includes the use of making available a standard number of personal computers for shared processing by personal computers; the network is connected to the World Wide Web and its successors; the personal user can override the means for maintaining a standard cost basis so that the personal user can obtain additional network services; the system has a control means by which to permit and to deny access to the personal computers by the network for shared computer processing; the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data

transmission that is at least greater than a peak data processing speed of the microprocessor.

Browsing functions generally include functions like those standard functions provided by current Internet browsers, such as Microsoft Explorer 3.0 or 4.0 and Netscape Navigator 3.0 or 4.0, including at least access to searching World Wide Web or Internet sites, exchanging E-Mail worldwide, and worldwide conferencing; an intranet network uses the same browser software, but may not include access to the Internet or WWW. Shared processing includes parallel processing and multitasking processing involving more than two personal computers, as defined above. The network system is entirely scalar, with any number of PC microprocessors potentially possible.

As shown in Figures **10A-10F**, to deal with operational and security issues, it may be beneficial for individual users to have one microprocessor or equivalent device that is designated, permanently or temporarily, to be a master 30 controlling device (comprising hardware and/or software and/of firmware and/or other component) that remains inaccessible (using, for example, a hardware and/or software and/or firmware and/or other component firewall 50) directly by the network but which controls the functions of the other slave microprocessors 40 when the network is not utilizing them.

For example, as shown in Figures **10A**, a typical PC 1 may have four or five microprocessors (even on a single microprocessor chip), with one master 30 and three or four slaves 40, depending on whether the master 30 is a controller exclusively (through different design of any component part), requiring four slave microprocessors 40; or the master microprocessor 30 has the same or equivalent microprocessing capability as a slave 40 and multiprocesses in parallel with the slave microprocessors 40, thereby requiring only three slave microprocessors 40. The number of PC slave microprocessors 40 can be increased to virtually any other number, such as at least about eight, about 16, about 32, about 64, about 128, about 256, about 512, about 1024, and so on. These multiples are not required, and the number of PC master microprocessors 30 may be increased. Also included is an internal firewall 50 between master 30 and slave 40 microprocessors. As shown in

preceding Figures 1-9, the PC 1 in Figure 10A may be connected to a network computer 2 and to the Internet or WWW or present or future equivalent or successor 3, like the Grid (or MetaInternet).

Other typical PC hardware components such as hard drive 61, floppy diskette drive 62, compact disk-read only memory (CD-ROM) 63, digital video disk (DVD) 64, Flash memory 65, random access memory (RAM) 66, video or other display 67, graphics card 68, and sound card 69, as well as digital signal processor or processors, together with the software and/or firmware stored on or for them, can be located on either side of internal firewall 50, but such devices as the display 67, graphics card 68 and sound card 69 and those devices that both read and write and have non-volatile memory (retain data without power and generally have to be written over to erase), such as hard drive 61, Flash memory 65, floppy diskette drive 62, read/write CD-ROM 63 or DVD 64 may be located on the PC user side of the internal firewall 50, where the master microprocessor is also located, as shown in Figure 10A, for security reasons; their location can be flexible, with that capability controlled such as by password-authorized access.

Alternately, any of these devices that are duplicative (or for other exceptional needs) like a second hard drive 61', can be located on the network side of the internal firewall 50. RAM 66 or equivalent or successor memory, which typically is volatile (data is lost when power is interrupted), should generally be located on the network side of the internal firewall 50, but some can be located with the master microprocessor to facilitate its independent use.

However, read-only memory (ROM) devices including most current CD drives (CD-ROM's) 63' or DVD's (DVD-ROM) drives 64' can be safely located on the network side of the internal firewall 50, since the data on those drives cannot be altered by network users; preemptive control of use may remain with the PC user.

However, at least a portion of RAM can be kept on the Master 30 microprocessor side of the internal firewall 50, so that the PC user can retain the ability to use a core of user PC 1 processing capability entirely separate from any network processing. If this capability is not desired, then the master 30 microprocessor can be moved to the network side of the internal firewall 50 and

replaced with a simpler controller on the PC 1 user side, like the master remote controller 31 discussed below and shown in Figure 10I.

The master microprocessor 30 may also control the use of several or all other processors 60 owned or leased by the PC user, such as home entertainment digital signal processors 70, especially if the design standards of such microprocessors in the future conform to the requirements of network parallel processing as described above. In this general approach, the PC master processor uses the slave microprocessors or, if idle (or working on low priority, deferable processing), makes them available to the network provider or others to use. Wireless connections 100, including optical wireless, are expected to be extensively used in home or business network systems, including use of a master remote controller 31 without (or with) microprocessing capability, with broad bandwidth connections such as fiber optic cable connecting directly to at least one component such as a PC 1, shown in a slave configuration, of the home or business personal network system; that connection links the home system to the network 2 such as the Internet 3, as shown in Figure **10I**. A business system may include broadband such as fiber optic or optical wireless links to most or all personal computers PC 1 and other devices with microprocessors, such as printers, copiers, scanners, fax machines, telephone and video conferencing equipment; other wired or wireless links also can be used.

A PC 1 user can remotely access his networked PC 1 by using another networked master microprocessor 30 on another PC 1 and using a password or other access control means for entry to his own PC 1 master microprocessor 30 and files, as is common now in Internet and other access. Alternately, a remote user can simply carry his own digitally stored files and his own master microprocessor or use another networked master microprocessor temporarily has his own.

In the simplest configuration, as shown in Figure **10B**, the PC 1 may have a single master microprocessor 30 and a single slave microprocessor 40, separated by an internal firewall 50, with both processors used in parallel or multitasking processing or with only the slave 40 so used, and connected with broad bandwidth such as optical fiber wire 99 to a network computer 2 and Internet 3 and successors like the Grid (or MetaInternet). Virtually any number of slave microprocessors 40 is

possible. The other non-microprocessor components shown in Figure 10A above may also be included in this simple Figure 10B configuration.

As shown in Figure 10C, microchips 90 are expected to integrate most or all of the other necessary computer components (or their present or future equivalents or successors), like a PC's volatile memory like RAM 66 (such as DRAM), graphics 82, sound 83, power management 84, network communications 85, and video processing 86, possibly including modem 87, non-volatile memory like flash (or magnetic like MRAM or ovonic unified memory) 88, system BIOS 88', digital signal processor (DSP) or processors 89, and other components or present or future equivalents or successors) and internal bus, on a single chip 90 (silicon, plastic, or other), known in the industry as "system on a chip". Such a PC microchip 90 can have the same architecture as that of the PC 1 shown above in Figure 10A: namely, a master control and/or processing unit 93 and one or more slave processing units 94 (for parallel or multitasking processing by either the PC 1 or the Network 2), separated by an internal firewall 50 and connected by broad bandwidth wire 99 such as optical fiber cable to a network computer 3 and the Internet 3 and successors like the Grid (or MetaInternet). Alternatively, microchip 90 can be an "appliance" system on a chip.

Existing PC components with mechanical components like hard drive 61, floppy or other removable diskette 62, CD-ROM 63, and DVD 64, which are mass storage devices with mechanical features that will likely not become an integral part of a PC "system of a chip" may still be capable of connection to a single PC microchip 90 and control by a single PC master unit 93.

In the simplest multi-processor case, as shown in Figure 10D, the chip 90 has a single master unit 93 and at least one slave unit 94 (with the master having a controlling function only or a processing function also), separated by an internal firewall 50 and connected by broad bandwidth wire 99 such as fiber optic cable to a network computer 3 and the Internet 3 (and successors like the Grid or MetaInternet). The other non-microprocessor components shown in Figure 10A above may also be included in this simple Figure 10D configuration.

As noted above, any computer may be both a user and provider, alternatively -- a dual mode operating capability. Consequently, any PC 1 within the network 2,

connected to the Internet 3 and successors like the Grid (or MetaInternet), can be temporarily a master PC 30 at one time initiating a parallel or multitasking processing request to the network 2 for execution by at least one slave PC 40, as shown in Figure **10E**. At another time the same PC 1 can become a slave PC 40 that executes a parallel or multitasking processing request by another PC 1' that has temporarily assumed the function of master 30, as shown in Figure **10F**. The simplest approach to achieving this alternation is for both master and slave versions of the parallel processing software to be loaded in each or every PC 1 that is to share in the parallel processing, so each PC 1 has the necessary software means, together with minor operational modifications, such as adding a switching means by which a signaled request for parallel processing initiated by one PC 1 user using master software is transmitted to at least a second PC 1, triggering its slave software to respond by initiating parallel processing.

As shown in Figures **10G** and **10H**, which are parallel to Figures 10E and 10F, the number of PC slave processors 40 can be increased to any virtually other number, such as at least about 4; as shown, the processing system is completely scalar, so that further increases can occur to, for example, about eight, about 16, about 32, about 64, about 128, about 256, about 512, about 1024, and so on; the PC master microprocessors 30 can also be increased.

In summary, as noted above relative to Figure 10I, a PC 1 can function as a slave PC 40 and be controlled by a master controller 31, which can be remote and which can have limited or no microprocessing capability, but can as well have similar or greater capability. As shown in Figures **10J** and **10K**, such a master controller 31 is located on the PC user side of the internal firewall 50, under the control of the PC user, while the microprocessors 40 reside on the network side of the internal firewall 50. The master controller 31 may receive input from the PC user by local means such as keyboard, microphone, videocam or future hardware and/or software and/or firmware or other equivalent or successor interface means (as does a master processor 40) that provides input to a PC 1 or microprocessor 30 originating from a user's hand, voice, eye, nerve or nerves, or other body part; in addition, remote access by telephone, cable, wireless or other connection may also be enabled by a hardware

and/or software and/or firmware and/or other means with suitable security such as password controlled access. Similarly, as shown in Figures **10L** and **10M**, relative to a PC "system on a chip", a master controller unit 93' (which could be capable of being accessed by the PC user through a remote controller 31) with only a controlling capability can be located on the PC user side of the internal firewall 50, under the control of the PC user, while the slave processor units 94 would reside on the network side of the internal firewall 50.

Figures **10N** and **10O** show PC 1 with an internal firewall 50 that is configurable through either hardware and/or software and/or firmware and/or other means; software configuration is easiest and most typical, but active motherboard hardware configuration is possible and may present some security advantages, including a use of manual or electromechanical or other switches or locks. Figure 10N shows a CD-ROM 63' that has been placed by a PC user on the network side of an internal firewall 50 from a previous position on the PC user side of an internal firewall 50, which was shown in Figure 10A. The settings of an internal firewall 50 may default to those that safely protect the PC 1 from uncontrolled access by network users, but with capability for the relatively sophisticated PC user to override such default settings and yet with proper safeguards to protect the unsophisticated user from inadvertently doing so; configuration of an internal firewall 50 may also be actively controlled by a network administrator in a local network like that of a business, where a PC user may not be the owner or leaser of the PC being used, either by remote access on the network or with a remote controller 31.

Similarly, Figures **10P** and **10Q** show a PC "system on a chip" 90 with an internal firewall 50 that is configurable through either hardware and/or software and/or firmware and/or other means; software configuration is easiest and most typical. Active configuration of the integrated circuits of the PC microchip 90 is also possible and may present some speed and security advantages. Such direct configuration of the circuits of the microchip 90 to establish or change its internal firewall 50 could be provided by the use of field-programmable gate arrays (or FPGA's) or their future equivalents or successors; microcircuit electromechanical or other switches or locks can also be used potentially. In Figure 10P, for example, slave

processing unit 94' has been moved to the PC user side of an internal firewall 50 from a network side position shown in Figures 10C and 10L. Similarly, Figure 10Q shows the same active configuration of chip circuit using FPGA's for the simplest form of multiprocessing microchip 90 with a single slave unit 94', transferring its position to the PC user's side of an internal firewall 50 from a network side shown in Figures 10M and 10D.

In summary, relative to the use of master/slave computers, Figures 10A-10I show embodiments of a system for a network of computers, including personal computers, comprising: at least two personal computers; means for at least one personal computer, when directed by its personal user, to function temporarily as a master personal computer to initiate and control the execution of a computer processing operation shared with at least one other personal computer in the network; means for at least one other personal computer, when idled by its personal user, to be made available to function temporarily as at least one slave personal computer to participate in the execution of a shared computer processing operation controlled by the master personal computer; and means for the personal computers to alternate as directed between functioning as a master and functioning as a slave in the shared computer processing operations. In addition, Figures 10A-10H show embodiments including those wherein the system is scalar in that the system imposes no limit to the number of personal computers; for example, the system can include at least 256 said personal computers; the system is scalar in that the system imposes no limit to the number of personal computers participating in a single shared computer processing operation, including at least 256 said personal computers, for example; the network is connected to the Internet and its equivalents and successors, so that personal computers include at least a million personal computers, for example; the shared computer processing is parallel processing; the network is connected to the World Wide Web and its successors; a means for network services, including browsing and broadcast functions, as well as shared computer processing such as parallel processing, are provided to said personal computers within said network; the network includes at least one network server that participates in the shared computer processing; the personal computers include a transponder or equivalent or successor

means so that a master personal computer can determine the closest available slave personal computers; the closest available slave personal computer is compatible with the master personal computer to execute said shared computer processing operation; the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data transmission that is at least greater than a peak data processing speed of the microprocessor; and a local network PC 1 being controlled remotely by a microprocessor controller 31.

Use of the internal firewall 50, as described above in Figures 10A-10I, provides a solution to a security problem by completely isolating host PC's 1 that are providing slave microprocessors to the network for parallel or other shared processing functions from any capability to access or retain information about any element about that shared processing. In addition, of course, the internal firewall 50 provides security for the host PC against intrusion by outside hackers; by reducing the need for encryption and authentication, the use of internal firewalls 50 can provide a relative increase in computing speed and efficiency. In addition to computers such as personal computers, the internal firewall 50 described above could be used in any computing device included in this application's above definition of personal computers, including those with "appliance"-type microprocessors, such as telephones, televisions or cars, as discussed above.

In summary, regarding the use of internal firewalls, Figures 10A-10I show embodiments of a system architecture for computers, including personal computers, to function within a network of computers, comprising: a computer with at least two microprocessors and having a connection means with a network of computers; the architecture for the computers including an internal firewall means for personal computers to limit access by the network to only a portion of the hardware, software, firmware, and other components of the personal computers; the internal firewall means will not permit access by the network to at least a one microprocessor having a means to function as a master microprocessor to initiate and control the execution of a computer processing operation shared with at least one other microprocessor having a means to function as a slave microprocessor; and the internal firewall means permitting access by the network to the slave microprocessor. In addition, the system

architecture explicitly includes embodiments of, for example, the computer is a personal computer; the personal computer is a microchip; the computer has a control means by which to permit and to deny access to the computer by the network for shared computer processing; the system is scalar in that the system imposes no limit to the number of personal computers, including at least 256 said personal computers, for example; the network is connected to the Internet and its equivalents and successors, so that the personal computers include at least a million personal computers, for example; the system is scalar in that the system imposes no limit to the number of personal computers participating in a single shared computer processing operation, including at least 256 said personal computers, for example; the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data transmission that is at least greater than a peak data processing speed of the microprocessor.

In summary, regarding the use of controllers with internal firewalls, Figures 10J-10M show embodiments of a system architecture for computers, including personal computers, to function within a network of computers, comprising for example: a computer with at least a controller and a microprocessor and having a connection means with a network of computers; the architecture for the computers including an internal firewall means for personal computers to limit access by the network to only a portion of the hardware, software, firmware, and other components of the personal computers; the internal firewall means will not permit access by the network to at least a one controller having a means to initiate and control the execution of a computer processing operation shared with at least one microprocessor having a means to function as a slave microprocessor; and the internal firewall means permitting access by the network to the slave microprocessor. In addition, the system architecture explicitly includes embodiments of, for example, the computer is a personal computer; the personal computer is a microchip; the computer has a control means by which to permit and to deny access to the computer by the network for shared computer processing; the system is scalar in that the system imposes no limit to the number of personal computers, including at least 256 said personal computers, for example; the network is connected to the Internet and its equivalents and

successors, so that the personal computers include at least a million personal computers, for example; the system is scalar in that the system imposes no limit to the number of personal computers participating in a single shared computer processing operation, including at least 256 said personal computers, for example; the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data transmission that is at least greater than a peak data processing speed of the microprocessor; and the controller being capable of remote use.

In summary, regarding the use of internal firewalls that can be actively configured, Figures 10N-10Q show embodiments of a system architecture for computers, including personal computers, to function within a network of computers, comprising for example: a computer with at least two microprocessors and having a connection means with a network of computers; the architecture for the computers including an internal firewall means for personal computers to limit access by the network to only a portion of the hardware, software, firmware, and other components of the personal computers; the internal firewall means will not permit access by the network to at least a one microprocessor having a means to function as a master microprocessor to initiate and control the execution of a computer processing operation shared with at least one other microprocessor having a means to function as a slave microprocessor; the internal firewall means permitting access by the network to the slave microprocessor; the configuration of the internal firewall being capable of change by a user or authorized local network administrator; the change in firewall configuration of a microchip PC is made at least in part using field-programmable gate arrays or equivalents or successors. In addition, the system architecture explicitly includes embodiments of, for example, the computer is a personal computer; the personal computer is a microchip; the computer has a control means by which to permit and to deny access to the computer by the network for shared computer processing; the system is scalar in that the system imposes no limit to the number of personal computers, including at least 256 said personal computers; the network is connected to the Internet and its equivalents and successors, so that the personal computers include at least a million personal computers; the system is scalar

in that the system imposes no limit to the number of personal computers participating in a single shared computer processing operation, including at least 256 said personal computers; the personal computers having at least one microprocessor and communicating with the network through a connection means having a speed of data transmission that may be at least greater than a peak data processing speed of the microprocessor.

PC 1 or PC general purpose microprocessors 90 may be designed homogeneously to the same basic consensus industry standard as parallel microprocessors for PC's (or equivalents or successors) as in Figures 10A-10B or for PC "systems on a chip" discussed in Figures 10C-10D. Although the cost per microprocessor might rise somewhat initially, the net cost of computing for all users is expected to fall drastically almost instantly due to the significant general performance increase created by the new capability to use of heretofore idle "appliance" microprocessors. The high potential for very substantial benefit to all users may provide a powerful force to reach consensus on industry hardware, software, and other standards on a continuing basis for such basic parallel network processing designs utilizing the Internet 3 and WWW and successors. Such basic industry standards may be adopted at the outset of system design and for use of only the least number of shared microprocessors initially. Such basic industry homogeneous standards may be adopted at the outset and for the least number of shared microprocessors initially, and design improvements incorporating greater complexity and more shared microprocessors may be phased in gradually over time on a step-by-step basis, so that conversion to the Grid (or MetaInternet) or architecture at all component levels may be relatively easy and inexpensive. The scalability of the Grid (or MetaInternet) system architecture (both vertically and horizontally) as described herein makes this approach possible.

By 1998, manufacturing technology improvements allow 20 million transistors to fit on a single chip (with circuits as thin as .25 microns) and, in the next cycle, 50 million transistors using .18 micron circuits. That entire computer on a chip may be directly linked by fiber optic or wireless optic or other broad bandwidth connection means to the network so that the limiting factor on data throughput in the

network system, or any part, may be only the speed of the linked microprocessors themselves, not the transmission speed of the network linkage. Such direct fiber or wireless optic linkage and integration of volatile memory (RAM like DRAM (dynamic random access memory) or equivalent), or non-volatile memory (like flash, magnetic, such as MRAM, or ovonic memory), on the "system on a chip" microchip obviates an increasingly unwieldy number of microchip connection prongs, which is currently in the three to four hundred range in the Intel Pentium and Pentium Pro series and will reach over a thousand prongs in the 1998 IBM Power3 microprocessor. One or more digital signal processors 89 and one or more all optical switches 92 located on a microprocessor 90 (or 30 or 40), together with numerous channels and/or signal multiplexing (such as wave division) of the fiber optic signal can substitute for a vast multitude of microchip connection prongs.

For computers that are not reduced to a single chip, the internal system bus or buses of any such PC's may have a transmission speed that is at least high enough that all processing operations of the PC microprocessor or microprocessors are unrestricted (and other PC components like RAM such as DRAM) and that the microprocessor chip or chips are directly linked by fiber optic or other broad bandwidth connection, as with the system chip described above, so that the limiting factor on data throughput in the network system, or any part, is only the speed of the linked microprocessors themselves, not the transmission speed of the linkage.

The individual user PC's may be connected to the Internet (via an Intranet)/Internet II/WWW or successor, like the Grid (or MetaInternet) network by any electromagnetic or optical means, such as with the very high transmission speed provided by the broad bandwidth of optical connections like fiber optic cable. Hybrid systems using fiber optic cable for trunk lines and coaxial cable to individual users may be used. Given the speed and bandwidth of transmission of fiber optic or equivalent or successor connections, conventional network architecture and structures should be acceptable for good system performance, making possible a virtual complete interconnection network between users.

However, the best speed for any parallel processing operation may be obtained, all other things being equal, by utilizing the available microprocessors that

are physically the closest together. Consequently, as shown previously in Figure 8, the network needs the means (through hardware and/or software and/or firmware and/or other component) to provide on a continually ongoing basis the capability for each PC to know the addresses of the nearest available PC's, perhaps sequentially, from closest to farthest, for the area or cell immediately proximate to that PC and then those cells of adjacent areas.

Network architecture that clusters PC's together is not mandatory and can be constructed by wired means. However, as shown in Figure 11, it may be very beneficial to construct local network clusters 101 (or cells) of personal computers 1' by wireless 100 means, especially optical wireless and dense wave division multiplexing (DWDM), since physical proximity of any PC 1 to its closest other PC 1' may be easier to access directly that way, as discussed further below. Since optical wireless range is about 3 kilometers currently, large clusters communicating with broadband connections are possible. In addition, at least several network providers may serve any given geographic area to provide competitive service and prices.

Those wireless PC connections may be PC-resident and capable of communicating by wireless or wired (or mixed) means with all available PC's in the cluster or cell geographic area, both proximal and potentially out to the practical limits of the wireless transmission.

As shown in Figure 12, wireless PC connections 100 can be made to existing non-PC network components, such as one or more satellites 110, or present or future equivalent or successor components and the wireless transmissions can be conventional radio waves, such as infrared or microwave, or can utilize any other part of the electromagnetic wave spectrum, particularly including optical, and can utilize dense wave division multiplexing (DWDM) to create numerous channels.

Moreover, as shown in Figure 13, such a wireless or wired approach also makes it possible to develop network clusters 101 of available PC's 1' with complete interconnectivity; i.e., each available PC 1 in the cluster 101 may be connected wirelessly 100 (including optical wireless and DWDM) to every other available PC 1 in the cluster 101, constantly adjusting to individual PC's becoming available or unavailable. Given the speed of some wired broad bandwidth connections, like fiber

optic cable, such clusters 101 with virtual complete interconnectivity is certainly a possible embodiment even for PCs with wired connections.

As shown in Figure **14A-14D**, such wireless systems may include a wireless device 120 comprising hardware and/or software and/or firmware and/or other component, like the PC 1 availability device described above resident in the PC, but also with a network-like capability of measuring the relative distance from each PC 1 in its cluster 101 by that PC's signal transmission by transponder or its functional equivalent and/or other means to the nearest other PC's 1' in the cluster 101. As shown in Figure 14A, this distance measurement could be accomplished in a conventional manner between transponder devices 120 connected to each PC in the cluster 101; for example, by measuring in effect the time delay from wireless transmission, optical or other and including DWDM, by the transponder device 120 of an interrogating signal 105 to request initiation of shared processing by a master PC 1 to the reception of a wireless transmission response 106 signaling availability to function as a slave PC from each of the idle PC's 1' in the cluster 101 that has received the interrogation signal 105. The first response signal 106' received by the master PC 1 is from the closest available slave PC 1" (assuming the simplest shared processing case of one slave PC and one master PC), which is selected for the shared processing operation by the requesting master PC 1, since the closer the shared microprocessor, the faster the speed of the wireless connections 100 is between sharing PC's (assuming equivalence of the connection means and other components among each of the PC's 1'). The interrogation signal 105 may specify other selection criteria also, for example, for the closest compatible (initially perhaps defined by a functional requirement of the system to be an identical microprocessor) slave PC 1", with the first response signal 106' being selected as above.

This same transponder approach also can be used between PC's 1" connected by a wired 99 (or mixed wired/wireless) means, despite the fact that connection distances would generally be greater (since not line of sight, as is wireless), as shown in Figure 14A, since the speed of transmission by broad bandwidth transmission means such as fiber optic cable is so high as to offset that greater distance. From a cost basis, this wired approach may be employed for such PC's already connected by

broad bandwidth transmission means since additional wireless components like hardware and software are not necessary. In that case, a functionally equivalent transponder device 120 may be operated in wired clusters 101 in generally the same manner as described above for PC's connected in wireless clusters 101. Networks incorporating PC's 1 connected by both wireless and wired (or mixed) means are anticipated, like the home or business network mentioned in Figure 10I, with mobile PC's or other computing devices using wireless connections. Depending on distances between PC's and other factors, a local cluster 101 of a network 2 may connect wirelessly between PC's and with the network 2 through transponding means linked to wired broad bandwidth transmission means, as shown in Figure 14C.

As shown in Figure 14D, the same general transponder device means 120 can also be used in a wired 100 network system 2 employing network servers 98 operated, for example, by an ISP, or in any other network system architectures (including client/server or peer to peer) or any other topologies (including ring, bus, and star) either well known now in the art or their future equivalents or successors.

The Figure 14 approach to establishing local PC clusters 101 for parallel or other shared processing avoids using network computers such as servers (and, if wireless, other network components including even connection means), so that the entire local system of PC's within a cluster 101 operates independently of network servers, routers, etc. Moreover, particularly if connected by wireless means, including optical wireless and DWDM, the size of the cluster 101 could be quite large, being limited generally by PC wireless transmission power, PC wireless reception sensitivity, and local and/or other conditions affecting transmission and reception. Additionally, one cluster 101 could communicate by wireless 100 means with adjacent, overlapping, or other clusters 101, as shown in Figure 14B, which could thereby include those beyond its own direct transmission range.

To improve response speed in shared processing involving a significant number of slave PC's 1, a virtual potential parallel processing network for PC's 1 in a cluster 101 may be established before a processing request begins. This is accomplished by the transponder device 120 in each idle PC 1, a potential slave, broadcasting by transponder 120 its available state when it becomes idle and/or

periodically afterwards, so that each potential master PC 1 in the local cluster 101 is able to maintain relatively constantly its own directory 121 of the idle PC's 1 closest to it that are available to function as slaves. The directory 121 may contain, for example, a list of about the standard use number of slave PC's 1 for the master PC (which initially probably is just one other PC 1") or a higher number, listed sequentially from the closest available PC to the farthest. The directory of available slave PC's 1 may be updated on a relatively up-to-date basis, either when a change occurs in the idle state of a potential slave PC in the directory 121 or periodically.

Such ad hoc clusters 101 should be more effective by being less arbitrary geographically, since each individual PC is effectively in the center of its own ad hoc cluster. Scaling up or down the number of microprocessors required by each PC at any given time is also more seamless.

The complete interconnection provided by such ad hoc wireless clusters is also remarkable because such clusters mimic the neural network structure of the animal brain, wherein each nerve cell, called a neuron, interconnects in a very complicated way with the neurons around it. By way of comparison, the global network computer described above that is expected in a decade can have at least about 10 times as many PC 's as a human brain has neurons and they can be connected by electromagnetic waves traveling at close to the speed of light, which is about 300,000 times faster than the transmission speed of human neurons (which, however, are much closer together).

As individual PC's continue to become much more sophisticated and more network oriented, compatibility issues may decrease in importance, since all major types of PC's will be able to emulate each other and most software, particularly relative to parallel processing, may no longer be hardware-specific. However, to achieve maximum speed and efficiency, it is beneficial to set compatible hardware, software, firmware, and other component standards to realize potential performance advantages attainable with homogeneous parallel processing components of the global network computer.

Until that compatibility or homogeneity is designed into the essential components of network systems, the existing incompatibility or heterogeneity of current components increases the difficulty involved in parallel processing across

large networks. Even so, the use of message passing interfaces (MPI) and parallel virtual machines (PVM), for example, has made massively parallel processing between heterogeneous personal computers fairly easy for uncoupled operations, as shown for example in the Beowulf operating system, Globus, and the Legion system, from which has been derived Applied Meta. Programming languages like Java provide a partial means for dealing with the heterogeneity problem, whereas Linux provides greater speed and efficiency. In addition, using similar configurations of existing standards, like using PC's available on the Internet (with its vast resources) with a specific Intel Pentium chip with other identical or nearly identical PC components is probably the best way in the current technology to eliminate many of the serious existing problems that can easily be designed around using available technologies by adopting reasonable consensus standards for homogeneous specification of all parallel processing system components, both networks and computers. The potential gains to all parties with an interest far outweigh the potential costs.

The above described global network computer system has an added benefit of reducing the serious and growing problem of the nearly immediate obsolescence of PC and other computer hardware, software, firmware, and other components. Since the system above is the sum of its constituent parts used in parallel processing, each specific PC component becomes less critical. As long as access to the network utilizing sufficient bandwidth is possible, then all other technical inadequacies of the user's own PC can be completely compensated for by the network's access to a multitude of technically able PC's of which the user will have temporary use.

Although the global network computer will clearly cross the geographical boundaries of nations, its operation is not likely to be unduly bounded by inconsistent or arbitrary laws within those individual states. There will be considerable pressure on all nations to conform to reasonable system architecture and operational standards generally agreed upon, since the penalty of potential exclusion from a global network computer system like the Internet/WWW is potentially so high as to not be politically possible any in any country.

As shown in Figure 15, because the largest number of user PC's are completely idle, or nearly so, during the night, it can be useful for the most complicated large scale parallel processing, involving the largest numbers of processors with uninterrupted availability as close together as possible, to be routed by the network to geographic areas of the globe undergoing night and to keep them there even as the Earth rotates by shifting computing resources as the world turns. As shown in the simplest case in Figure 15, during the day, at least one parallel processing request by at least one PC 1 in a network 2 in the Earth's western hemisphere 131 is transmitted by very broad bandwidth connection wired 99 means such as fiber optic cable to the Earth's eastern hemisphere 132 for execution by at least one PC 1' of a network 2', which is idle during the night, and the results are transmitted back by the same means to network 2 and the requesting at least one PC 1.

Any number of individual PC's within local networks like that operated by an ISP can be grouped into clusters or cells, as is typical in the practice of the network industry. As is common in operating electrical power grids and telecommunications and computer networks, many such processing requests from many PC's and many networks could be so routed for remote processing, with the complexity of the system growing substantially over time in a natural progression.

Alternatively, for greater security or simplicity, nighttime parallel processing can remain within a relatively local area and emphasize relatively massively parallel processing by larger entities such as business, government, or universities for relatively complicated applications that benefit from comparatively long nightly periods of largely uninterrupted use of significant numbers of slave personal computers PC 1.

Any of the embodiments shown in Figures 1-15 can be combined with one or more of any other of Figures 1-15 of this application to provide a useful improvement over the art.

While the conventional approach to configuring a network of personal computers PC 1 for parallel processing is simply to string them together in a simple bus-type architecture, as shown previously in Figure 9, Figures **16A-16Z** and **16AA** show a new hierarchical network topology.

Although the Figure 9 network structure is simple and produces reasonable results in loosely coupled problems like geographic searches described earlier, as a general approach it has at least three important problems.

First, as the number of personal computers PC 1 being used in the network grows, an increasingly greater deal of complex pre-operation planning and custom tailoring-type programming at the master PC 1 level is required to establish a means for allocating portions of the operation among the large number of available personal computers PC 1'.

Second, operational results coming back to PC 1 from personal computers PC 1' are not synchronized, so that PC 1 frequently alternates between being idle and being overwhelmed. When the number of personal computers PC 1' is very large, both problems can be significant; when the number is massive, the problems can be overwhelming and seriously degrade the operation of the network.

Third, generally there are no means established for personal computers PC 1' to communicate or cooperate with each other during such network operations, so sharing operational results during processing between personal computers PC 1' is usually not feasible, especially when large numbers of PC 1 are involved. Consequently, closely coupled problems are generally not amenable to solution by conventional parallel processing by computers using a simple bus-type network like Figure 9.

The new hierarchical network topology shown in Figure 16A is a simple subdivision step whereby a personal computer PC 1 (or equivalent PC on a microprocessor chip 90) or microprocessor 30 acting as a master M_1 divides a given operation into two parts (for example, two halves), then sends by an optical or electrical connection such as optical fiber or wire 99 the one half parts to each of two connected available slave personal computers PC 1 (or PC microprocessor 90) or microprocessor 30, as shown one processing level down as S_{21} and S_{22}. The topology of Figure 16A (and subsequent Figures 16) can be connected to the Internet 3 and World Wide Web, for example.

Figure 16B shows that slave personal computer PC 1 (or PC microprocessor 90) or microprocessor 40 located at S_{21} has temporarily adopted the same functional

role as a master to repeat the same subdivision of the given operation. Therefore, having already been divided in half once in Figure 16A, the given operation is again subdivided in Figure 16B, this time in half into quarters of the original operation (for example) by S_{21}, which then sends one quarter to each of two additional available slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 located at S_{31} and S_{32}.

Figure 16C shows personal computers PC 1 (or PC microprocessor 90) or microprocessors 40 at S_{31} and S_{32} sending operational results back to S_{21} after performing the processing required by the given operation, instead of repeating again the subdivision process. That processing action by S_{31} and S_{32} can be dictated by pre-established program criteria, for example by automatically defaulting to operational processing at the S_3 level after two subdivision processes as shown above, so that the operation can be processed in parallel by four available slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40. Alternately, as another example, the criteria can be a user preference command overriding an otherwise automatic default to level three processing in order to specify some other level of processing involving more or less slave PC 1 (or PC microprocessors 90) or microprocessors 40.

Similarly, in Figure 16A above, the personal computer PC 1 (or PC microprocessor 90) or microprocessor 40 acting as master M_1 also can initiate the parallel processing operation (or, alternatively, a multi-tasking operation) on the basis of preset program parameters through software, hardware, or firmware or other means; parameter examples again may be pre-set automatic default or user preference override.

Like Figure 16C, Figure 16D shows operational results being passed back to the next higher level, this time from slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40, S_{21} and S_{22}, to master personal computer PC 1 (or PC microprocessor 90) or microprocessor 30, M_1, where the operation is completed after the S_{21} and S_{22} results are consolidated.

Figure 16G shows master personal computer PC 1 (or PC microprocessor 90) or microprocessor 30, M_1, offloading by wireless connection 100, such as optical

wireless and DWDM for example, the entire parallel processing operation to an available slave personal computer PC 1 (or PC microprocessor 90) or microprocessor 40 that temporarily functions as S_1 in the place of M_1 on the first processing level for the duration of the given parallel processing (or multi-tasking) operation, the first step of which the operation is shown in Figure 16H, which is like Figure 16A except as shown.

Figure 16I shows a personal computer PC 1 (or PC microprocessor 90) or microprocessor 40 that is executing a command to function in the slave role of S_{21} for a given operation but has become unavailable, or was unavailable initially (due, for example, to interruption for another higher priority command by its user or to malfunction), when results of the given operation from a lower parallel processing level are passed to S_{21}. In that situation, S_{21} (or S_{31} or S_{32}) can simply offload those results to another personal computer PC 1 (or PC microprocessor 90) or microprocessor 30 (or 40) that is then available and it can become S_{21} and take over the role of S_{21} in the given operation for the duration of that operation. Similarly, the role of any unavailable or malfunctioning master or slave PC 1 or microprocessor 90, 30, or 40 can be transferred to an available functioning one.

As shown in Figure 16J, S_{21} then completes the parallel processing operation and passes its portion of the operational results to M_1.

The offloading capability of functional roles of master and slave personal computers PC 1 (and PC microprocessors 90) and microprocessors 30 (and 40) from unavailable to available PC 1, 30 and 40 as shown in Figures 16G-16J can also be used in previous figures in this application. In the simplest case initially, all processing roles of personal computers PC1 (and PC microprocessors 90) and microprocessors (30 or 40), like S_{21}, above can be determined at the beginning of an operation based on availability (based on non-use and lack of malfunctioning component) and remain unaltered until the end of the operation. But, with more sophisticated system software and hardware and firmware, during an operation any number of the processing roles can be offloaded from personal computers PC 1 (or PC microprocessors 90) or microprocessors 30 (or 40) to others as required, even multiple times and many simultaneously.

Figure 16E shows the multi-processing network topology of Figures 16A-16J in a larger scale embodiment, including all personal computers PC 1 (or PC microprocessors 90) or microprocessors 30 (or 40) that are participating in a typical operation, including in this example one personal computer PC 1 (or PC microprocessor 90) or microprocessor 30 (or 40) at level one; two at level two; four at level three; and eight at level four. The network topology is completely scalar in that any practical number of additional processing levels or personal computers PC 1 (or PC microprocessors 90) or microprocessors 30 (or 40) can be added to those shown. Topologies limited to just two (or three) levels are also possible, which is the simplest case of operation processing subdivision that distinguishes over the conventional Figure 9 single level "string-together" architecture.

The number of processing personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 doubles at each additional processing level and therefore can be represented by 2^N, where N is the last or final processing level, for the simplest case, as shown above, which is splitting one given operation into two parts such as halves between each level.

Instead of subdividing one operation as above, two separate parallel processing operations can be multi-tasked on separate branches, such as S_{21} and S_{22} as shown, using the same network architecture described above. As is clear from this example, any practical mix of multi-tasking and/or parallel processing is possible using the above network architecture.

Figure 16E shows the distribution of a given parallel processing (or multi-tasking) operation as routed through a four level virtual network, beginning at M_1. "Virtual" as used here means temporary, since in the next parallel operation originating at M_1 it may be the case that many of the personal computers PC 1 (or microprocessors 90) or microprocessors 30 (or 40) that had been available for a previous operation would not still be available for the next operation.

Figure 16E shows a binary tree network architecture for the initial distribution of an operation from M_1 down through four slave processing levels, while Figure 16F shows the subsequent processing and accumulation of results back from there to M_1. Figure 16F shows an inverted view of Figure 16E to show the sequence of the

operation, from operation distribution in Figure 16E to result accumulation in Figure 16F.

More specifically, Figure 16F shows the processing slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 at the fourth level, S_{41} through S_{48}, where they process the operation to produce results which are then routed back through two other levels of the virtual network to M_1.

In the routing of operational results shown in Figure 16F, each slave personal computer PC 1 (or PC microprocessor 90) or microprocessor 40 has the capability to either simply pass through those results only as a direct communication link or connection; or, alternatively, for example, to consolidate those results sent from the personal computers PC 1 (or PC microprocessor 90) or microprocessors 40 at a lower level; or, to provide additional other processing based on those lower processing level results.

Such consolidation or additional processing can reduce or eliminate duplicative data from a search or other operation producing duplicative results and can also serve to buffer the originating master M_1 from overloading caused by many sets of results arriving at M_1 in the Figure 9 single processing level architecture in an uncoordinated fashion from what may be a large number of slave personal computers PC 1 (or PC microprocessor 90) or microprocessors 40. Such a consolidation role for personal computers PC 1 (or PC microprocessor 90) or microprocessors 40 substantially reduces or eliminates the excessive custom pre-planning and synchronization problems of the conventional Figure 9 network topology discussed above.

Figure 16K shows a simple example indicative of the extremely complicated network structure that can result from subdividing a given operation in which the complexity of the operation involved is not uniform, due to, for example, variations in the data. In this example, pre-set program splitting criteria can be employed that balances the processing load of each slave personal computer PC 1 (or PC microprocessor 90) or microprocessor 40. With this approach, the complex portions of a given operation can automatically draw greater resources in the form of additional splitting of that more difficult portion of the problem, so that additional

levels of parallel processing slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 can be brought into the virtual network to process the operation, as shown in the left branch of Figure 16K.

Figure 16K is a fairly simple example, but when the same kind of dynamic network structure is applied to a virtual network using many more personal computers PC 1 (or PC microprocessor 90) or microprocessors 30 or 40 and many processing levels, involving both micro levels in PC microprocessor chips 90 and macro levels in personal computers PC 1 networks (such as shown later in Figure 20B), then the potential complexity of the virtual network increases significantly. For example, each PC microprocessor chip 90 may have 64 slave microprocessors 94 on the final processing level; each personal computer PC 1 may have 64 slave PC microprocessor chips 90 at the final processing level, and the virtual network may include 64 personal computers PC 1 at the final processing level. With this large number of physical resources available (which can of course be very substantially greater) to the virtual network created by processing a given operation or operations, like that shown in Figure 16K, it is clear that the operation itself can sculpt an incredibly complex virtual network that is custom tailored to the specific operation. All that is required is a operation subdivision process as described earlier that can be resident in each PC 1 (or PC microprocessor 90) or microprocessor 30 or 40, or that can be passed along with data (as can be operation application software) as the operation is executed.

Thus, Figure 16K shows an example of a highly flexible virtual network architecture that is capable of being dynamically configured in real time by the processing requirements imposed on the components of the network by a specific given operation and its associated data, as allowed by the network hardware/software/firmware architecture.

Figures 16L and 16M show examples of other possible subdivision parallel processing methods, such as subdivision routing to three slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 at the next level down, as shown in Figure 16L, or subdivision routing to four slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40, as shown in Figure 16M. Subdivision

routing to any practical number of slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 between processing levels can be done.

Such routing subdivision can also vary between processing levels or even within the same processing level, as shown in Figure 16N; these exemplary variations can result from pre-set program criteria such as those that balance operational loads, like those shown previously in Figure 16K. The means for subdividing problems for parallel or multi-tasking processing can also vary, within at least a range of methods known in the computer and mathematical arts.

Figure 16O shows slave personal computer PC 1 (or PC microprocessor 90) or microprocessor 40, S_{41}, sending operational results to a higher processing level, S_{31}, which can then function as a router or as one or more high speed switch 42 (which can be located as 92 on a PC microprocessor 90 also, including as an all optical switch), passing through unaltered results back down to the original level to personal computer PC 1 (or PC microprocessor 90) or microprocessor 40, S_{42}, as shown in Figure 16P. Figure 16Q demonstrates the capability for any two pair of slave personal computers PC 1 (or PC microprocessors 90) or microprocessors 40 like S_{41} and S_{42} to communicate directly between each other, including wired or wirelessly 100 as shown. Figures 16O-16Q show the same subsection of the network topology shown in Figure 16F (the left uppermost portion).

A personal computer PC 1 (or PC microprocessor 90) or microprocessor 30 (or 40) located on a higher processing level in the network architecture such as S_{31} can process results as well as route them, as shown in Figure 16V, in which S_{31} receives results from S_{41} and S_{42} at a lower processing level and then processes that data before sending its processing results to a higher level to S_{21}, as shown in Figure 16W.

Together, Figures 16V-16W and 16O-16Q show the capability of any personal computer PC 1 (or PC microprocessor 90) or microprocessor 30 (or 40) of the Figure 16F (and 16E) network structural and functional invention to communicate with any other personal computer PC 1 (or PC microprocessor 90) or microprocessor 30 (or 40) participating in a given parallel processing (or multi-tasking) operation. That

communication can take the form of simple pass-through of unmodified results or of modification of those results by processing at any level.

Figures 16X-16Z show the applicant's new hierarchical network structure and function applied to the design of a personal computer PC 1, as discussed previously in Figures 10A and 10B. Figure 16X shows the simplest general design, with a master M_1 microprocessor 30 and two slave S_{21} and S_{22} microprocessors 40. Figure 16Y shows the same network structure with an additional level of slave microprocessors 40, S_{31} through S_{34}, while Figure 16Z shows the same network structure as Figure 16Y with an additional level of slave microprocessors 40, S_{41} through S_{48}. As shown in these examples, this network structure is completely scalar, including any practical number of slave microprocessors 40 on any practical number of processing levels.

Figure 16AA shows a useful embodiment in which each microprocessor 30 and 40 has, in addition to internal cache memory, its own random access memory (RAM) 66 or equivalent memory (volatile like DRAM or non-volatile like Flash memory, magnetic such as MRAM memory, or ovonic unified memory), integrated on-microchip 90 or separate off-microchip. A significant amount of such microchip RAM (volatile like DRAM or non-volatile like Flash memory, magnetic such as MRAM memory, or ovonic unified memory), significantly greater than cache memory (SRAM) and other on-chip memory used on microprocessor chips today, can be beneficial in improving the efficient operation of the microprocessor; if located off microprocessor chip, the size of such memory can substantially exceed the size of the associated microprocessor, but an on-microprocessor chip location for DRAM or Flash (or MRAM or ovonic memory), like cache (SRAM) memory, offers the best potential for improving microprocessor speed and efficiency. The design can also incorporate (or substitute) conventional shared memory or RAM 66' (i.e. memory used by all, or some, of the microprocessors 30 or 40 (or 90) of the personal computer PC 1).

Figures 16R-16T are parallel to Figures 16X-16Z above, but show PC microprocessor 90 architecture rather than macro PC 1 architecture; a PC microprocessor 90 is as earlier described in Figure 10C, a personal computer on a microchip.

Figure 16U is like Figure 16AA, also except for showing PC microprocessor 90 architecture instead of PC 1 architecture. Figure 16U shows a useful embodiment in which each PC microprocessor 93 or 94 has its own integrated on-microchip (or separate off microchip) random access memory (RAM) 66 or equivalent memory (volatile like DRAM or non-volatile, like Flash memory, magnetic such as MRAM memory, or ovonic unified memory). A significant amount of such RAM or other memory, significantly greater than cache (SRAM) memory or other on-microchip memory used on microprocessor chips today, can be beneficial in improving the efficient operation of the microprocessor; if located off-microprocessor chip, the size of such memory can substantially exceed the size of the associated microprocessor, but an on-microprocessor chip 90 location for DRAM or Flash (or MRAM or ovonic memory), like cache (SRAM) memory, offers the best potential for improving microprocessor speed and efficiency. The microchip design can also incorporate (or substitute) conventional shared memory or RAM 66' (i.e. memory used by all, or some, of the PC microprocessors 93 or 94 of the personal computer PC microprocessor 90).

Figures 16R-16U show a different and improved basic microchip architecture which can exclude or reduce the currently used superscalar approach in microprocessors to execute multiple instructions during each clock cycle. The Figures 16R-16U architecture is much simpler and, by integrating memory with microprocessor, reduces memory bottlenecks. The simplicity of the Figures 16R-16U microchip design, which may have little or no superscalar components, compared to conventional superscalar designs (the inherent extreme complexity of which creates a very substantial memory overhead), can result in the use of a much greater proportion of independent, non-superscalar processors per microchip, exclusive of integrating memory or RAM 66 onto the microprocessor chip 90, as discussed in Figure 16U.

Figures 16X-16Z and 16AA, by using the same architecture for PC 1 networks as Figures 16R-16U, import the same advantage of microchip parallel processing performance to parallel processing in PC 1 networks.

Figure 16AB shows a direct connection of optical fiber 99 from Internet 3 (or another network) to random access memory (RAM) microchip 66'. The connection

may be at a central portion 140 of RAM chip 66' to provide equal access to stored data on RAM chip 66'. The direct connection can be anywhere on RAM chip 66'. Digital signal processor (DSP) 89 is on RAM chip 66' for connection with optical fiber 99. RAM chip 66' is for shared memory use among PC's 1 and for broadcast use. RAM chip 66' can include volatile or non-volatile (flash-type) memory. RAM chip 66' can have more than one DSP 89, such as shown in Figure 20B.

All Figures 16A-16Z and 16AA-16AB, like the preceding figures of this application, show sections of a network of personal computers PC 1 (or PC microprocessors 90) or microprocessors 30 or 40 which can be parts of the WWW or Internet or Internet II or the Next Generation Internet (meaning connected to it) or Intranets or Extranets or other networks.

Also, except for Figures 16R-16T and 16X-16Z, all of the Figure 16 series show personal computers PC 1 and microprocessors 30 or 40 as occupying the same location. This dual representation was done for economy of presentation and to show the parallel functionality and interchangability in conceptual terms of personal computer PC 1 and microprocessors 30 or 40 in the structure of the new network. So, taking Figure 16A as an example, M_1, S_{21} and S_{22} show three personal computers PC 1 or, alternatively, one microprocessor 30 and two microprocessors 40.

As noted initially in Figure 10C, a personal computer PC 1 can be reduced in size to a PC microprocessor chip 90, so preceding Figures showing personal computer PC 1 also generally represent PC microprocessor chip 90.

Finally, Figures 16A-16Z and 16AA-16AB show a mix of electrical and optical connections, including wired 99, especially connections such as optical glass fiber or omniguides, and wireless 100, especially wireless optical (and mixtures of both in a single figure), and dense wave division multiplexing (DWDM). Generally, either 99 or 100 or a mix can be used relatively interchangeably in the network inventions shown (as well as in prior figures), though in some embodiments either highest transmission speed (i.e. broadest bandwidth) or mobility (or some other factor) may dictate a use of wired or wireless. Generally, fiber optic wire 99 and dense wave division multiplexing (DWDM) may provide the most advantageous transmission means because it has the greatest bandwidth or data transmission speed,

so it may be used for connections between personal computers and microchips, including direct connections, although optical wireless 100 also offers very high bandwidth, especially with dense wave division multiplexing (DWDM). Other wireless 100 (but also including optical wireless), including with DWDM, can be used where mobility is a paramount design criteria.

The Figure 16 embodiments can be combined with, or modified by incorporating, any other network system architectures (including client/server or peer to peer) or any other topologies (including ring, bus, and star) either well known now in the art or their future equivalents or successors.

Any of the embodiments shown in Figures 16A-16Z and 16AA-16AB can be combined with any one or more of the preceding or subsequent figures of this application to provide a useful improvement over the art.

The parallel processing network architecture shown in the preceding Figures 16A-16Z and 16AA-16AB and in earlier figures has several features unique to its basic design that provide for the security of personal computers PC 1 (or PC microprocessor 90) or microprocessor 40 that share other computers for parallel and multi-tasking processing. First, the slave personal computers PC 1 (or microprocessors 40) each have only part of the operation (for large operations, only a very small part) and therefore unauthorized surveillance of a single PC 1 can provide only very limited knowledge of the entire operation, especially in only a relatively local area in which switching or routing was employed. Second, the addresses of the slave personal computers PC 1 (or microprocessors 40) are known or traceable, and therefore are not protected by anonymity (like hackers usually are) in case of unauthorized intervention. In addition, cryptography can be employed, with on microprocessor chip 30, 40, or 90 hardware 55 being used in some embodiments due to efficiency, although software and firmware can also be used, or a separate PC 1 hardware-based component 56 like an encryption microchip can be used; with either encryption component 55 or 56, micro electromechanical locks can be used to prevent access other than by the direct physical user; other MicroElectroMechanical System (MEMS) devices located on microchips like PC90 can be used for access prevention

or other functions. Nonetheless, these inherent strengths can be substantially reinforced, as indicated in Figures **17B-17D**.

Figure 17A shows at least one internal firewall 50 performing its conventional function of keeping out intruders such as hackers from the Internet 3 from unauthorized access for either surveillance of, or intervention in, a user's personal computer PC 1 (or PC microprocessor 90) or master microprocessor 30.

Figure 17B shows that, since Internet users can, as enabled by the applicant's network structure invention, use one or more of the slave microprocessors 40 of another's personal computer PC 1 (or PC microprocessor 90) for parallel (or multi-tasking) processing, the at least one internal firewall 50 has a dual function in also protecting Internet 3 use (or other shared use on a network) from unauthorized surveillance or intervention by a PC 1 owner/user who is providing the shared resources. To maintain the privacy necessary to operate such a cooperatively shared network arrangement, unauthorized surveillance or intervention must be carefully prevented by hardware/software /firmware or other means.

Figure 17C therefore shows master M personal computer PC 1 (or PC microprocessor 90) using the slave S_2 microprocessor 40 of a different personal computer, PC 1', which is available for Internet 3 (or other net) shared use, while internal firewall 50' blocks unauthorized access into PC 1' by PC 1 (although PC 1' owner/user can always interrupt a shared operation and take back control and use of slave S' microprocessor 40, which then triggers off-loading action to compensate, as discussed above in Figures 16I-16J).

Figure 17D is similar to Figure 17C, but shows a PC microprocessor 90 with a slave microprocessor 94 being used by Internet 3 users (or other net), so that at least one firewall 50 serves both to deny access such as surveillance by master M microprocessor 93 to an Internet 3 parallel processing (or multi-tasking) operation on slave S microprocessor 94 and to deny access to master M microprocessor 93 by Internet 3 (or other net) users of slave S microprocessor 94. At least one internal firewall 50 may be implemented by non-configurable hardware at the microchip level to provide protection against tampering with the internal firewall 50 by a PC 1 user, who has easier access to software or macro hardware such as PC motherboards to

alter. PC 90 microchips may employ tamper-resistant construction or tamper-proof construction. As such, PC 90 microchips may be permanently locked by out-of-specification conditions or permanently destroyed by attempts at physical access.

Also, non-configurable hardware denying access from the network is the most immune to hacking from any outside source, including the Internet, and can therefore be used either for general protection or to protect an innermost kernel of the most confidential of personal files (such as passwords or financial data) and the most critical of operating system components, such as the system bios or access to file alternation.

At the same time, the Figure 17 and earlier embodiments provide a solution to digital rights management by providing a highly safe environment for the owners of digital versions of audio, video, and software copyrighted material. Such copyrighted material as movies, television, music, and application or operating system software may be decrypted and controlled on the network user side of the PC 1 or PC 90, while the PC 1 user is denied access to the decrypted digital version of the copyrighted material. However, the network user can make the material viewable to the PC 1 user, but not copyable, via the PC 1 and PC 90 microchip architecture shown in Figures 10A and 10C.

Any of the embodiments shown in Figures 17A and 17B can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

The flexible network architectures shown earlier in Figure 16K and other Figure 16 series (and other figures) have many applications and may be used to design improvements and alternatives to the network itself. In addition, the flexible network can be used to simulate and design personal computers PC 1 and particularly PC microprocessor chips 90 (and other microchips), which may be static or configurable (in response to the requirements of a given operation, like the Figure 16K network architecture) or a mix.

The Figure 16K network architecture has capabilities that substantially exceed simulating the fairly simple binary circuit structure of a typical PC microprocessor 90 or other microchip, since any personal computer PC 1 or PC microprocessor chip 90

in the Figure 16K network can simulate much more than a simple binary circuit on/off state or other simple microchip circuit. Any PC 1 or PC microprocessor chip 90 in a Figure 16K network can represent virtually any number of states or conditions simulating any kind of circuit, however complex it might be, the only limit being the processing time required for what can be a very large number - thousands or millions - of personal computers PC 1 or PC microprocessors 90 to process the simulation; there are only practical constraints, not theoretical ones, although increasingly large numbers of processors are expected to be phased in, as discussed before.

One potential related application of prior described network inventions is to simulate the unique "qubit" component necessary to construct a quantum computer, as well as a virtual quantum computer itself.

Figures **18A-18D** show designs for a virtual quantum computer or computers. Figure 18A shows personal computer PC 1 (or microprocessor 90) with the addition of a software program 151 simulating a "qubit" for a quantum computer or computers and thereby becoming a virtual qubit (VQ) 150, a key component of a quantum computer 153. Figure 18B shows a personal computer PC 1 (or microprocessor 90) with a digital signal processor (DSP) 89 connected to a hardware analog device 152 simulating a qubit, with the PC 1 monitoring the qubit through the DSP 89, thereby simulating a virtual qubit (VQ) 150 for a quantum computer 153; this arrangement allows the option of simultaneous use of the PC 1 through multi-tasking for both digital and quantum computing.

Figure 18C is like Figure 16A, but incorporates a virtual qubit in PC 1, so that a virtual quantum computer 153 can have any network architecture like those shown in Figures 16A-16Z and 16AA-16AB, as well as other figures of this application.

As shown in Figure 18D, for example, a virtual qubits (VC) 150 network can provide complete interconnectivity, like Figure 13. Virtual qubits VC 150 like those described in Figures 18A & 18B can be added to or substituted for microprocessors 30 and 40 in prior Figures 16B-16Q and 16V-16AA of this application, as well as earlier figures. As shown by those prior figures, the number of virtual qubits 150 is limited only to whatever is practical at any given time; in terms of development, that means as few as a single qubit 150 in one or more networked personal computers PC

1 to begin, but the number of qubits 150 may become extremely large, as indicated in previous figures. Figure 18D shows a mix of wired 99 and wireless 100 connections.

Any of the embodiments shown in Figures 18A-18D can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Like personal computers located in the home or office, personal computers PC 1 in automobiles 170 (including other transportation vehicles or other conveyances) are in actual use only a very small percentage of the time, with the average dormant period of non-use totaling as much as 90 percent or more. Personal computers PC 1 are now being added to some automobiles and will likely become standard equipment over the next decade or so. In addition, automobiles already have a very large number of microcomputers on board in the form of specialized microprocessors 35 which are likely to become general parallel processors in future designs, as discussed earlier in this application.

Automobiles therefore form a potentially large and otherwise unused resource for massive parallel processing through the Internet 3 and other networks, as described in earlier figures. However, when idle and thus generally available for network use, automobiles lack their usual power source, the engine, which of course is then off, since it is too large to efficiently provide electrical power to on board computers, except occasionally. As shown in Figure 19, the car engine can have a controller (hardware, software or firmware or combination in the PC 1 or other microprocessor 35), for example, connected to an automobile computer network 178 to automatically start the automobile engine in order to recharge the car battery 171 when the battery is low (and well before the battery is too low to start the engine), but the engine additionally needs to be controlled as above not to expend all available fuel automatically.

Alternately, the automobile 170 can be fitted with a very small auxiliary engine-power electrical power generator 177 to provide power to the automobile's computer network; the engine of the generator 177 can be fed by the main engine fuel tank and controlled as above.

Two solutions, not mutually exclusive, to alleviate (but not solve) the lack of power problem noted above are, first, adding an additional car battery 171' for network use (at least primarily) or, second, using a single battery but adding a controller in the PC 1, for example, that prevents the existing battery 171 from being discharged to a level near or below that which is needed to start the automobile 170.

In addition, as shown in Figure 19, one or more solar power generating cells or cell arrays 172 can be incorporated in an automobile's outer surface, with generally the most effective placement being on a portion of the upper horizontal surface, such as a portion of the roof, hood, or trunk. For charging the automobile battery 171 when sunlight is not available, such as at night or in a garage, a focused or focusable light source 173 can provide external power to the solar panel.

Alternately, a connection device 174 such as a plug for an external electrical power source can be installed on or near the outer surface of the automobile. In addition, or independently, a connection device 175 for an optical fiber (or other wired) external connection to the Internet 3 or other net may be used; an intermediate high transmission speed can also exist between the automobile network and a fiber optic connection to the Internet 3. Alternately, a wireless receiver 176, including optical wireless and/or DWDM, located near where the automobile is parked, such as in a garage, can provide connectivity from the automobile's personal computer or computers PC 1 directly to the Internet 3 or to a network in a home or business like that shown in Figure 10I.

Any of the embodiments shown in Figure 19 can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Figure 20A is like Figure 16Y (and can be combined with Figure 16AA), but in addition shows a slave microprocessor 40 functioning as S_1, the function of master having been temporarily or permanently offloaded to it by M_1 microprocessor 30. In addition, Figure 20A shows the processing level of slave microprocessors 40, S_{31} through S_{34}, each with a separate output/input communication link to a digital signal processor (DSP) 89 or other transmission/ reception component; the transmission linkages are shown as 111, 112, 113, and 114, respectively. The DSP 89 can be

connected to a wired 99 means such as optical fiber to the Internet (or other net), although non-optical fiber wire can be used (and probably does not require a DSP 89).

Figure 20B is like Figure 16S (and can be combined with Figure 16U), but with the same new additions described above in Figure 20A. Like Figure 16S, Figure 20B shows a detailed view of personal computer PC microprocessor 90_1, which is a personal computer PC on a microchip 90, including two more levels of parallel processing within the microprocessor 90. In addition, the two new levels of PC microprocessor 90 shown in Figure 20B are a second processing level consisting of PC microprocessors 90_{21} through 90_{24} and a third processing level consisting of PC microprocessors 90_{31} through 90_{316} (a third level total of 16 microprocessors 90). Each of the three processing levels shown in the Figure 20B example is separated between levels by an intermediate direct connection to the Internet 3 (or other network) and by four output lines from the higher processing level. For example, microprocessors 90_{21} through 90_{24} are shown receiving respectively from the outputs 111 through 114 from four slave microprocessors 94, S_{31} through S_{34} of PC microprocessor 90_1.

PC microprocessor 90_1 is shown in detail including all slave microprocessors 94, while other PC microprocessors 90 at the second and third processing levels are not, for simplicity and conciseness of presentation. An additional processing level can be present, but is not shown for the sake of simplicity, and personal computers PC 1 like Figure 20A can be used interchangeably with PC microprocessors 90.

Figure 20B shows that between each processing level the output links from every PC microprocessor 90 can be transmitted from slave microprocessors 94 directly to PC microprocessors 90 at the next processing level below, such as from PC microprocessor 90_{21} down to PC microprocessors 90_{31} through 90_{34}, via the Internet 3 or other net. Each of the transmission/ reception links from those slave processing microprocessors 94 (S_{31} through S_{34}), shown as 111, 112, 113, and 114 for PC microprocessor 90_1, can be transmitted or received on a different channel (and can use multiplexing such as wave or dense wave division, abbreviated as DWDM) on an optical fiber line (because of its huge capacity, one optical fiber line is expected to be sufficient generally, but additional lines can be used) that may connect directly to PC

microprocessor chip 90_1, which can incorporate a digital signal processor 89 or other connection component (of which there can be one or more) for connecting to the wired connection like fiber optic line, as shown, or wireless connection.

Any of the embodiments shown in Figures 20A and 20B can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Figures 21A and 21B are like Figures 20A and 20B (and therefore also can be combined with Figures 16AA and 16U, respectively), but show additionally that all microprocessors 30, 40, 93, and 94 of PC 1 or PC 90_1 can have a separate input/output communication link to a digital signal processor (DSP) or other transmission/ reception connection component. The additional communications linkages are shown as 141, 142, 143, and 144, which connect to M_1, S_1, S_{21}, and S_{22}, respectively, and connect to the network, including the Internet 3, the WWW, the Grid, and equivalents or successors. Like all preceding and subsequent figures, Figures 21A and 21B are schematic architectural plans of the new and unique components of the parallel processing system invention disclosed in this application and can represent either physical connections or virtual relationships independent of hardware. Figure 21B shows an embodiment in which the additional linkages lead through the Internet 3 to microprocessors PC 90_{25}-90_{28}.

The additional communications linkages 141, 142, 143, and 144, as well as the original linkages 111, 112, 113, and 114 of Figures 20A and 20B, may have a bandwidth sufficiently broad to at least avoid constraining the processing speed of microprocessors 30, 40, 93, and 94 connected to the linkages. The ultra high bandwidth of optical connections like optical fiber or omniguides or optical wireless may provide external connections between PC 1 and PC 90_1 microprocessors that are far greater than the internal electrical connections or buses of those microprocessors, for example, by a factor of 10, or 100, or 1000, which are already possible with optical fiber, or 1,000,000, which is possible with optical omniguides, which are not limited to a relatively smaller band of wavelengths using DWDM like optical fiber; future increases will be substantial since the well established rate of increase for optical bandwidth is much greater than that for microprocessor speed and electrical

connections. Wireless optical antennas that are positioned on the exterior of houses, buildings, or mobile reception sites, instead of inside of glass or other windows, should significantly increase the number of optical wavelengths that can be sent or received by each of the wireless optical antennas; the entire connection is freespace optical wireless, which allows for greater dense wave division multiplexing (DWDM) and thereby greater bandwidth.

A major benefit of the embodiments shown in Figs. 21A-21B is that PC 1 and PC 90_1 can function like the Figure 9 embodiment to efficiently perform operations that are uncoupled, so that each microprocessor M_1, S_1-S_{34} can operate independently without microprocessors M_1, S_1, and S_{21}-S_{22} being idled, as they may be in Figures 20A and 20B. Another benefit is that for tightly coupled parallel operations, microprocessors M_1, S_1, and S_{21}-S_{22} can have broad bandwidth connections with microprocessors 30, 40, 93, or 94 that are not located on PC 1 or PC 90_1. Thus the embodiments shown in Figures 21A and 21B provide an architecture that allows PC 1 or PC 90_1 the flexibility to function in parallel operations either like Figures 20A-20B embodiments or like the Figure 9 embodiment, depending on the type of parallel operation being performed. Studies indicate that single chip multiprocessors like PC 90_1 can also perform uniprocessor operations with a speed like that of uniprocessor architectures like wide-issue superscalar or simultaneous multithreading.

Like Figures 20A and 20B, the embodiment of Figures 21A and 21B includes broad bandwidth connection to the Internet 3 by wired means such as optical connection by fiber optic cable or omniguide or optical wireless, although other wired or non-wired means can be used with benefit, and the use of DWDM or wideband CDMA is clearly advantageous. It should be noted that the architecture of the Figure 20 and 21 embodiments may be particularly advantageous with ultrawideband communication connections.

Another advantage of the embodiments shown in Figures 22A and 22B when functioning in the Figure 9 form of loosely coupled or uncoupled parallel processing or multitasking is that if PC 1 or PC 90_1 is functioning as a web server and typically uses only one microprocessor to do so, it can quickly add mirror web sites using one or more additional microprocessors to meet increasing volume of visits or other use of

the web site. This replication of web sites on additional microprocessors in response to increasing load can also be done using the Figure 16 form of tightly coupled parallel processing. PC 1 and PC 90_1 or any of their microprocessors 30, 40, 93, and 94 or other components can also serve as a switch or a router, including other associated hardware/software/firmware network components.

Any of the embodiments shown in Figures 21A and 21B can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Binary tree configurations of microprocessors shown in Figures 16, 20, 21A, and 21B can be laid out in 2D using an H-tree configuration, as shown in **Figure 21C**, and can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Figure 22A shows a microprocessor PC 90_1 like that of Figure 21B, except that Figure 22A shows the microprocessors 93 and 94 each connecting to an optical wired interconnection 99' such as thin mirrored hollow wire or omniguide or optical fiber (and other very broad bandwidth connections can be used); the interconnect can include a digital signal processor 89' employed with a microlaser 150, which can be tunable, and other components to transmit and receive digital data for microprocessors 93 and 94 into the optical wired interconnects 99' such as an omniguide using, for example, a specific wavelength of light for each separate channel of each separate microprocessor 93 and 94 utilizing dense wave division multiplexing (DWDM).

Figure 22B shows an enlargement of the digital signal processor 89' with microlaser 150 with other transmission and reception components.

Figure 22A shows a simple bus network connection architecture between the interconnect 99' and the microprocessors 93 and 94. However, since the interconnection 99' is optical and the bandwidth available is very broad, the optical connection 99' allows connections between microprocessors 93 and 94 in PC 90_1 that are functionally equivalent to those shown in Figure 21B, which includes a representation of physical connections. The interconnects between microprocessors 93 and 94 like Figure 21B are shown within the omniguide 99' shown in Figure 22A. In fact, the potential bandwidth of the optical interconnect 99' is so great that

complete interconnection between all microprocessors 93 and 94 with PC 90_1 is possible, even for a much greater number of microprocessors either in a larger PC 90_1, like Figure 16T for example, or in other PC 90s, such as PC 90_{21}-90_{24} and 90_{31}-90_{316} in Figures 20B and 21B connected to PC 90_1 through a network such as the Internet 3, the WWW, or the Grid; consequently, any conventional network structure can be implemented. Consequently, the embodiment shown in Figure 22A has the flexibility of those of Figures 21A and 21B to function in parallel operations like either the Figures 20A-20B embodiments or like the Figure 9 embodiment, depending on the type of parallel operation to be performed; or the Figure 16 embodiments.

It should be noted that the optical interconnect 99' shown in Figure 22A can beneficially have a shape other than a thin wire or tube, such as an omniguide with any form or shape located above and connection to microlasers 150 at a suitable location such as on or near the upper surface of the microchip PC 90_1 located at least at each microprocessor 93 and 94 or connected thereto, for example; the optical interconnect 99' and microlasers 150 and associated transmission and reception components can be located elsewhere on the microchip PC 90_1 with benefit. An omniguide can take a waveform shape or rely exclusively on a mirrored (or semi-mirrored) surface or surfaces (or combination of both shape and mirrored surface) to guide lightwave signals such as propagated by a microlaser 150 substantially directly and/or by reflection. A relatively large optical interconnect 99' can enable freespace or wireless-like connections between microlasers 150; such an optical interconnect 99' can cover substantially the entire PC90 microchip or can connect multiple PC90 microchips and can connect one or more PC90 microchips to other PC components.

As shown in Figure 22A, random access memory (RAM) 66 can be located on microchip PC 90_1 like in Figure 16U and also can be connected directly or indirectly to the optical interconnect 99' (or use non-optical connections not shown), so that the microprocessors 93 and 94 and RAM 66 can communicate with a very broad bandwidth connection, including with RAM 66 and microprocessors 93 and 94 located off microchip PC 90_1 on the network including the Internet 3 and WWW. Any other component of the PC 90 microchip can be connected with the optical interconnect 99' and more than one such interconnect 99' can be used on the same PC

90 or other microchip. Microlasers 150 can include, for example, 5-to-20-micron-high (or other height) vertical cavity-surface-emitting lasers (VCSELs), which can beam down waveguides built into the PC90 microchip; alternatively, freespace optics can be employed; and lenses can be employed. Radio-frequency (RF) signals can also be used for similar interconnects 99'. Micro light emitting diodes (LEDs) can substitute for one or some or all of the microlasers 150 and either can be a transceiver (transmit and receive light signals).

Figure 22C is a side cross section of the microchip PC 90_1 shown in Figure 22A taken at hatched line 22C (which is abbreviated). Figure 22C shows the location of the omniguide above the surface of the microprocessors 93 and 94 and RAM 66 and connecting them while also containing two or more microlasers 150 (associated DSP and other components not shown) proximate to each to contain the optical signal generated by the microlasers 150 so that the signal can be transmitted between microprocessors 93 and 94 and RAM 66 either directly or by being reflected off the mirrored (or semi-mirrored) surface of the omniguide 99', for example. Each of the microprocessors 93 and 94 (or 30 or 40) and RAM 66 (or any other memory component such as L1 cache or L2 cache, for example, or other microchip component) can have one or more microlasers 150 and each such microlaser 150 can distinguish itself from other microlasers 150 on the microchip (or off it) that also generate wavelength signals by using, for example, a distinct wavelength of light for data transmission and/or utilizing wave or dense wave division multiplexing. Figure 22A is a top view of the microchip PC 90_1, which is a PC system on a microchip, any of which disclosed in this application can be also more generally any microchip with multiple processors. The microlasers 150 (and associated transmission and reception components such as DSP) that are associated with RAM (or parts of it) or other memory components can either provide data in response to direct inquiries or fetches made by a microprocessor 93 or 94 or can broadcast a continual stream of current data (continually updated and repeated in continuous cycle, for example) which is used by the microprocessor as needed.

Any of the embodiments shown in Figures 22A, 22B and 22C can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Figure 23A shows multiple firewalls 50, a concept indicated earlier by the at least one firewall 50 discussed in Figure 17D. Figure 23A shows a PC1 or microchip 90 with a primary firewall 50 and additional interior firewalls 50^1, 50^2, and 50^3, that are within primary firewall 50. As shown, interior firewall 50^3 is in the most protected position, since it is inside all the other firewalls, while the other interior firewalls 50^2, and 50^1 are progressively less protected, since, for example, interior firewall 50^1 is protected from the outside network only by the primary firewall 50. As shown, progressively more protected positions can be created within the PC1 or microchip 90. The interior firewalls can also be arranged in any other way within the primary firewall 50. The interior firewalls can be used to separate user files from system files, for example, or to separate various hardware components from each other. In this manner, a number of compartments can be created within the PC1 or microchip 90 to more safely protect the software, hardware, and firmware of the PC1 or microchip 90, just as ships have a number of separate watertight compartments to protect against flooding and avoid sinking. Any of the primary or interior (or other inner firewalls discussed below) can be hardware, software, or firmware, or a combination, and can coexist in layers, so that a firewall 50, for example, may have a hardware firewall, a software firewall, and a firmware firewall, either as independent units or as integrated components. W^3 in Figure 23A and subsequent Figures denotes the World Wide Web.

Figure 23B shows another embodiment of compartments created by inner firewalls within a PC1 or microchip 90. Primary firewall 50 and interior firewall 50^1 are like Figure 23A, but interior firewalls 50^2, 50^3, and 50^4 are shown perpendicular to firewalls 50 and 50^1 (just to illustrate in a simplified schematic way, which may be different in an actual embodiment). In this way, an upper row of compartments U^1 and U^2 can be used, for example, to bring from the network files which are first authenticated and then enter into the U^1 compartment, are decrypted, and undergo a security evaluation, such as by virus scan, before transfer to the most secure

compartment U^2. Any operations could potentially occur in any compartment, depending on the level of security desired by the user (by over-ride) for example, but an advantageous default system would allow for files with the highest levels of authentication, encryption, and other security evaluations to be allowed into the most secure compartments.

Similarly, operating system files can also be authenticated and brought from the network side of the PC1 or microchip 90 into compartment O^1 for decryption and security evaluation or other use, and then finally transferred into the most secure compartment O^2. Again, similarly, a row of compartments can be used for separating hardware, such as a master microprocessor 30 or 93 being located in compartment M^1 and a remote controller 31, for example, located in compartment M^2.

Also, additional inner firewalls 50^{22}, 50^{33}, and 50^{44} can be located outside the primary firewall 50, but within the network portion of the PC1 or microchip 90, to separate user files in compartment U from operating system files in compartment O from hardware such a slave microprocessor in compartment S on the network side. In the example shown, an additional row is shown for hardware, including a hard drive in a compartment HD on the network side, a hard drive in compartment HD^1 on the PC1 or microchip 90 user's side, and flash memory (such as system bios 88) in compartment F^2. Each microprocessor 30, 40, 93, or 94 can have its own compartment in a manner like that shown in Figure 23B, as can associated memory or any other hardware component.

Figure 23C shows an inner firewall 50 embodiment similar to Figure 23B, but Figure 23C shows that any file or set of files, such as operating files O or user data files U or application files A, can have its own inner firewall 50^O or 50^U or 50^A. Similarly, any hardware component, such as hard drive HD, also can have its own inner firewall 50^{HD}. Additionally, more than one file or set of files or hardware components can be grouped together within an inner firewall, such as 50^S shown in Figure 23C.

Figures 23D and 23E show operating system files O or application files A like those shown in Figure 23C, but organized differently in discrete layers, each separate grouping of the operating or application files having a separate firewall 50

(and optionally with as well as a PC1 or PC90 firewall shown in earlier Figures), so that the firewall structure is like that of an onion. The operating system files O or application files A can have a parallel structure, with an innermost kernel operating system or application file located in the center, with additional features in other files in subsequent layers, from the simplest to the most complex and from the most secure and trusted to the least secure and trusted.

Using this structure, as shown in **Figure 23D**, an innermost operating system core O^1 may be firmware stored in a read-only memory (ROM), located in a microchip for quick access, so that a simplest version operating system with all core features can be protected absolutely from alteration and can be available almost immediately, without lengthy boot up procedures required by loading the operating system from a hard drive, for example. The core operating system O^1 can include a core of the system BIOS or of the operating system kernel, for example; it would be advantageous for this core to be capable of independent operation, not dependent on components in other levels to operate at the basic core level (similarly, other levels can advantageously be independent of higher levels).

A secondary operating system O^2 can be software located advantageously on flash or other microchip non-volatile memory such as magnetic (or less advantageously, a hard drive or other mechanical storage media) and can consist of additional features that are more optional, such as those not always used in every session, or features that require updating, changing, or improving, such features coming from trusted sources located on a network, such as the Internet or the Web; additional portions of or upgrades to the system BIOS and the operating system kernel can be located in O^2, for example.

A third level operating system O^3 located, for example, on a hard drive, can consist of additional software features that are used only occasionally and are more optional, and can be loaded as needed by a user into DRAM or magnetic memory microchip for execution, for example. Operating systems O^2 and O^3 can include, for example, the most recent upgrades from a known and trusted source, such as a commercial software vendor or open source software developer, that are downloaded from a network, including the Internet and the Web, or loaded from conventional

memory media like CD or floppy diskette. All three levels of such operating systems O^1, O^2, and O^3 together can constitute, for example, roughly the equivalent of a conventional PC operating system typical in the year 2000.

A fourth level operating system O^4, for example, can consist of special use or single use operating system add-ons, especially software coming from untrusted or unauthenticated sources on a network, such as the Internet or the Web.

For example, the graphical interface of the operating system can be in 2D only at the O^1 level, in 3D at the O^2 level, rendering at the O^3 level, and animation in the O^4 level; additionally, a standard format can be maintained in the O^1 and O^2 levels, with user or vender customization at the O^3 level.

As shown in **Figure 23E**, application files such as A^1, A^2, A^3, and A^4 can be structured the same way as operating system files O in Figure 23D and with the same layered approach to firewalls 50 as in Figure 23D. Typical application software of the year 2000 can be restructured in this manner.

The kernel operating system files O^1 and O^2, as well as kernel application files A^1 and A^2 can be located in any personal computer PC1 or PC90, including at the level of an appliance including the simplest device, advantageously in ROM and in non-volatile read/write memory such as Flash (or magnetic such as MRAM, or ovonic memory) microchips, for example, as described in Figures 23D and 23E above. Inclusion of wireless connection capability is advantageous, as is the use of DWDM.

An advantage of the file and firewall structures shown in Figures 23D and 23E is that a system crash or file corruption should never occur at the simple and unalterable level O^1 or A^1 and any level above O^1 or A^1 can be recovered at a lower level, specifically the highest level at which there is a stable system or uncorrupted data. For example, a word processing application program can have the most basic functions of a typewriter (i.e. storing alphanumeric, punctuation, spacing, and paragraph structure data) stored on a ROM microchip in A^1 and related user files (i.e. such as a word document) on U^2. Insertion of a digital video file into a word document can be handled at the A^3 level and insertion of a downloaded special effect at the A^4 level. In this example, a crash caused by the insertion at the least secure and most complex A^4 level would not disturb the word document located at the U^2 or U^3

level. Rebooting and/or recovery can be automatic when detected by the operating system or at the option of the user.

Thus, Figures 23A-23E illustrate embodiments wherein a PC1 or microchip 90 includes a hierarchy of firewalls. In the context of the present invention, firewalls may be structured to allow varying degrees of access from the network side of PC1 or microchip 90. As discussed above, ROM may totally deny access from the network side, effectively creating an innermost firewall. Hardware, software, firmware, or combinations thereof may be structured to deny or allow a predetermined maximum level of access from the network side, effectively creating outer firewalls. Similarly, intermediate firewalls effectively may be created.

The embodiments of Figures 23A-23E, as well as earlier Figures 17A-17D and earlier embodiments, provide a solution to digital rights management by providing a highly safe environment for the owners of digital versions of audio, video, and software copyrighted material. Such copyrighted material as movies, television, music, and application or operating system software may be decrypted and controlled on the network user side of the PC 1 or PC 90, while the PC 1 user is denied access to the decrypted digital version of the copyrighted material. However, the network user can make the material viewable to the PC 1 user, but not copyable, via the PC 1 and PC 90 microchip architecture shown in Figures 10A and 10C. For example, a copyrighted movie or music album may be a file that is associated with control and other software; all files located on one or more specific hardware components may be grouped together within an inner firewall, such as 50^S shown in Figure 23C.

Additional security for copyright owners may be provided by using a digital signal processor (DSP), and/or analog and/or other components grouped within the inner firewall 50^S to convert network user selected decrypted digital files into analog files before they are transmitted off the PC 90 microchip, so that only an analog signal exits the PC 90 microchip for viewing or listening by the PC 1 user. As such, direct digital copying by the PC 1 user of copyrighted digital files provided over the Internet is prevented.

Any of the embodiments shown in Figures 23A-23E can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

Additionally, an inner firewall can divide any hardware component into a separate network side compartment and a separate firewall protected side compartment. For example, a hard drive 61 can have a controller 61' that is divided into two compartments, HD and HD^1, as above. As shown in **Figure 24**, the user side HD^1 compartment of the controller 61' can have a read capability controller r and a write capability controller w, while the network side HD compartment can be limited to a read capability controller r only. The user side HD^1 compartment controller can be, for example, used to control only the upper surface of the hard drive 61 platters, while the network side HD compartment controller can be used to control only the lower surface of the hard drive 61 platters, so that a single hard drive can effectively serve a dual role as both a network-accessible hard drive and a user-accessible hard drive, while maintaining a firewall 50 between them. Additionally, the network side HD controller can optionally have a write capability also, which can be preemptively turned on or off by the PC1 or microchip 90 user. Other relative allocations between network and user of the HD 61 platters can be made and can be configurable by the user or system administrator or not configurable.

Similarly, CD drives 63 or DVD drives 64 (read only or read/write) can have a controller 63' or 64' like that of the HD controller 61' above that is divided by a firewall 50, so that some laser beams are under network control and other laser beams are under user control, like the above hard drives. Floppy disk drives, "Zip" drives, and other removable disk or diskette drives can similarly be divided by a firewall 50 so that there is a physical user portion of the disk or diskette and a physical network portion of the disk or diskette, both either fixed or configurable by a user or system administrator or other authorized source. Memory microchips such as RAM or Flash or other can also be divided into network and user sides in a similar manner.

Any of the embodiments shown in Figure 24 can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

The use of volatile memory on the network side of the PC1 or microchip 90 is particularly useful in eliminating viruses and other security problems originating from the network side, such as malicious hackers on the Internet. When the network side of the firewall 50 of the PC1 or microchip 90 is returned to its user (preemptively or otherwise), volatile memory like random access memory (RAM) such as DRAM on the network side can first be erased. For example, volatile memory can be purged by momentarily interrupting power to the network side of the PC1 or microchip 90, thereby erasing all network data so that no network data is retained when the user regains control of the network side of the PC1 or microchip 90 for the user's use, except at the user's option; other conventional means may be employed. Of course, when the user is specifically using the network side, for example, for Web browsing, the operating system or the user can selectively save network side files or transfer them to the user side.

On the network side, non-volatile memory like Flash, MRAM, and ovonic memory with network data must be overwritten to obtain the same erasure-type protection, which can be a disadvantage if it takes much more time. Moreover, for relatively large storage media, such as CD-RW or DVD-RW with write-once capability, network data writing must be tracked to be effectively erased. Any new network file on non-volatile memory with only a write-once capability can be erased by overwriting all "0's" to "1's", so that, for example, the network data written on a CD-RW or DVD-RW would be converted to all "1's" or "pits" (no unpitted writing surface within the network data sector, permanently overwriting the file); optionally, the operating system or the user can selectively save network side files or transfer them to the user side, or vice versa. There is a disadvantage to using Flash memory, since repeated overwriting will eventually degrade it.

Figures 25A-25D show the use for security of power interruption or data overwrite of volatile memory like DRAM and non-volatile memory like Flash or MRAM (or ovonics), respectively, of the network portion (N) of a personal computer PC1 or system on a microchip PC90; the network (N) portion being created within a PC1 or PC90 by a firewall 50 (as described above in previous figures) and including resources that, when idled by a user, can be used by the network, including the

Internet (I) or the World Wide Web. Such use is to prevent the unplanned or approved mixture of user and network files by either files being retained in the "swing space" (N) during the transition from use by a network user to use by the PC1/PC90 user or vice versa.

As shown in Figure 25A and Figure 25C, when the network portion (N) of the PC1 personal computer or PC90 microchip is idled by a user, for example, power is interrupted to volatile memory like DRAM and/or data is overwritten to files in non-volatile memory like Flash or MRAM (or ovonics), so that no files exist in the network portion (N) after such interruption or overwriting.

After the step shown in Figures 25A and 25C, the network portion (N) can be used safely from a security viewpoint by a user from the network, including the Internet and the World Wide Web (and potentially including other network resources), as shown in Figure 25B, or by the PC1/PC90 user, as shown in Figure 25D, potentially including other resources from the user portion (U) of the PC1 or PC90. As noted earlier, the Figure 25 approach can advantageously be used as an additional feature to other conventional security measures.

Any of the embodiments shown in Figures 25A-25D can be combined with one or more of any of the preceding figures of this application to provide a useful improvement over the art.

The PC 90 microchip as previously described, or a personal computer PC 1 (or any microchip, including a special or general purpose microprocessor on a microchip, alone or including one or more other system components as previously described) may include one or more photovoltaic cells 201, as are well known in the art. The photovoltaic cells 201 may be located on the PC 90 microchip or located near the PC 90 microchip, such as adjoining it or adjacent to it, or located less near, such as in the PC 90 microchip user's home, office, or vehicle, either inside or outside, or may be located more remotely.

Figure 26A shows one or more photovoltaic cells 201 located on a PC 90 microchip. The photovoltaic cells 201 may use electromagnetic radiation, such as visible light, as a power source that is directed to the cells 201 by an optical waveguide 202, which may include a size that is sufficient to allow the cells 201 to generate

electrical power at maximum output level or at a most efficient level. In addition, visible light in freespace (without a waveguide 202) may also serve as a power source and can be directed by the use of one or more lenses 204.

Figure 26B shows a single microchip 200 including both a PC 90 and one or more photovoltaic cells 201. Figure 26B shows a top view of a multi-layer microchip having one or more photovoltaic cells 201 on one side of a microchip 200, with a PC 90 on the other side of the microchip 200, as shown in **Figure 26C** in a bottom view of the same microchip as Figure 26B. Besides being integrated on the same microchip 200, the photovoltaic cells 201 may be located separately from the PC 90 microchip, and the two separate elements may be joined or adjoining.

A light source for the photovoltaic cells 201 can be direct or indirect and can be sunlight or artificial light, including light from a laser, or a combination, and can be optionally focused by a lens 204. The light may be coherent with one or more discrete frequencies, such as from a laser, or incoherent with many frequencies. The artificial light may be generated by well known conventional means that are conventionally powered by electricity distributed by the existing electrical power grid, as is well known in the art.

A single photovoltaic cell or a number of cells 201 may power each component on the PC 90 microchip, such as the master microprocessor 93 or slave microprocessors 94, DRAM or MRAM, Flash memory, DSP, or laser 150, or any of the other components previously described. The photovoltaic cells 201 may be connected to one or more batteries. The photovoltaic cells 201 can be located remotely as a separate unit, such as on the PC 90 microchip user's roof at home, car, or office, so that the cells 201 provide general local power or power dedicated to the PC 90 microchip and/or associated components. The PC 90 microchip may be a network server, router, or switch, so that any network component can be powered by photovoltaic cells 201, including the Internet, an Intranet, or the World Wide Web.

The Figure 26A-26C embodiments advantageously eliminate the need for a microchip, such as the PC 90 microchip, to have a wired connection 99 that typically provides power or data or both, but which also provides a connection means for the entry of electromagetic flux, which can impair or destroy the functioning of the PC 90

microchip. The embodiments shown rely on light, which does not transmit electromagnetic flux, for power and data.

Figure 27A shows a single microchip 200, combining a PC 90 microchip (or any microchip, including a special or general purpose microprocessor on a microchip, alone or including one or more other system components as previously described) and one or more photovoltaic cells 201, that is substantially surrounded by a Faraday Cage 300, such as is well known in the art, that is optimized to shield against magnetic flux, including high frequency flux (and may include shielding against electric flux). Faraday Cage 300 may be constructed of a mesh structure, or may also be a continuous structure without holes, which has an advantage of preventing entry by very high frequency electromagnetic flux, and may incorporate other microchip structures, such as a heat sink 301.

Figure 27B shows separate PC 90 microchip and one or more photovoltaic cells 201; the two separate components are connected by a wire 99, and all three components are substantially surrounded by a Faraday Cage 300, also known as a Faraday Shield or Screen.

Figure 27C shows the same components as Figure 27B, but shows each component substantially surrounded by a separate Faraday Cage 300, all of which may be connected. For portable handheld wireless devices, the ground for the Faraday Cage 300 may be the user's body.

As shown in **Figure 27D**, the PC 90 microchip may be located in a housing for any of the PC's described previously, such as a case of a laptop personal computer 401 or a PC cell phone 402, which may also have a separate Faraday Cage 300, so that the PC 90 microchip is substantially surrounded by more than one Faraday Cage 300. The inner Faraday Cage 300 surrounding the PC 90 microchip may be optimized to shield against specific frequencies of magnetic flux, such as high frequency flux in the microwave range, which may be assisted by the relatively smaller size of the PC 90 microchip (compared to its housing). Figure 27D shows an inner Faraday Cage 300 surrounding only a portion, the PC 90, of a microchip such as the combined microchip 200.

As shown in **Figures 27E and 27F**, the PC 90 microchip can be separate from the photovoltaic cell or cells 201 and can be joined by a wired connection 99.

As shown in **Figure 27E**, an inner Faraday Cage 300 may surround only a portion of a PC 90 microchip, such as a Magnetic Random Access Memory (MRAM) component.

Figure 27F shows Faraday Cage 300 that surrounds only a portion of one or more photovoltaic cells 201, such as a part conducting an electrical current flow directly to the PC 90 microchip.

The PC 90 microchip may also be powered by one or more fuel cells 211 or one or more batteries (each with one or more cells) 221 or any combination of such batteries 221, fuel cells 211, or photovoltaic cells 201. As shown in **Figures 27E and 27F**, the PC 90 microchip is typically separate from a fuel cell or cells 211 or batteries 221 and can be joined by a wired connection 99, as shown, as is the case with a photovoltaic cell or cells 201. A wired connection 99 can be configured to protect the PC 90 microchip from electromagnetic flux through the use of RF traps or Ferrite grommets or beads 212 on the wire or cable connection 99.

By providing power without an external wired connection 99, both fuel cells 211 and batteries 221 isolate the PC 90 microchip from a power grid that can transmit electromagnetic flux, but to do so a battery or batteries 221 can be configured to provide connection to the power grid only intermittently when charging is required.

Figure 27G shows a microchip, such as a PC 90 microchip, surrounded by a Faraday Cage 300 but without including a photovoltaic cell 201 shown in Figures 27A-27F.

Figure 27H shows a PC housing such as a laptop PC 401 or PC cell phone 402 including a PC 90 microchip and separate Faraday Cages 300 surrounding both the microchip and housing. Also shown is an antenna 499 (or antennas) for wireless communication that can be separated from the Faraday Cage 300 to protect the electrical components of the PC by an RF trap or Ferrite grommets or beads 212. The antenna 499 can project externally from the PC housing or be located internally in the PC housing, such as in the screen housing of a laptop PC 401. In an exemplary implementation, the antenna 499 is located outside of at least one Faraday Cage 300.

Any of the embodiments shown in Figures 26A-26C and 27A-27H may be combined with one or more other embodiments shown in those figures or in preceding Figures 1-25 and described herein.

It is currently contemplated that commercial embodiments of the networks, computers, and other components of the Internet, World Wide Web, and the Grid (or MetaInternet) described in this application in the preceding Figures 1-25, including hardware, software, firmware, and associated infrastructure will be developed in conjunction and with the assistance of the Internet Society (ISOC), the World Wide Web Consortium (W3C), the Next Generation Internet (NGI), professional organizations like the Institute of Electrical and Electronics Engineers (IEEE) and the American National Standards Institute (ANSI), as well as other national and international organizations, and industry consortia drawn from the telecommunication, T.V. cable, ISP, network, computer, and software industries, as well as university and other research organizations, both U.S. and international, to set agreed upon operating standards which, although often arbitrary, are critical to efficient, reliable functioning of the Grid (or MetaInternet).

It is also presently contemplated that the Linux programming language will take a central role in the Grid (or MetaInternet), since a homogeneous system has an advantage as being most efficient and effective, and Linux is among the most stable, efficient higher level software available, one that has already established a preemininent role in distributed parallel processing. A heterogeneous Grid (or MetaInternet) is certainly feasible too, but less advantageous, as is the Java programming language, which excels in heterogeneous environments. Although Linux may be employed instead of Java in keeping with the more effective homogeneous approach for parallel processing systems that can scale even to the massive numbers of PCs available on the Internet and WWW, either Java or principles employed in Java may be used with benefit, especially in certain cases like security, such as the use of "sandboxes" to provide secure execution environments for downloaded code (see page 39 of The Grid, Foster and Kesselman and associated bibliography references 238, 559, 555, and 370), although use of one or more internal firewalls as discussed earlier in Figures 10 and 17 to protect personal user files and

critical hardware and software systems, such as the operating system, may provide similar capability.

It is also contemplated currently that, like the Linux programming language, the Grid (or MetaInternet) described in this application can be developed into a commercial form using open source principles for Internet-like standards for software and hardware connections and other components. Such open source development is anticipated to be exceptionally successful, like Linux, because much of it can be freeware, although modified with one vital enhancement to provide equity for significant contributors: minimal licensing fees that are to be paid only by medium to large commercial and governmental entities at progressive rates based on financial size; the resulting funding can be used for significant financial and other awards for special research and development efforts relating to the Grid (or MetaInternet) and its open source development, particularly outstanding achievements by individuals and teams, especially independent developers and virtual teams, the awards also being progressive in terms of importance of contribution and most being peer-selected. Open source commercial development of the Grid (or MetaInternet) should therefore, like Linux, attract the most interested and best qualified technical expertise on the planet, all linked by the Internet and WWW to collaborate virtually in realtime 24 hours a day and 7 days a week, creating a virtual entity extraordinarily skilled in the existing art.

It is also anticipated that the exclusive rights to the Grid (or MetaInternet) granted by patents issued on this application, particularly for the homogeneous embodiment of the Grid (or MetaInternet) - which is by far the most effective and efficient form - will ensure that the Grid (or MetaInternet) is homogeneous on critical hardware and software standards and protocols. That is because any heterogeneous systems cannot compete commercially due to inherent inferiority in efficiency, while any competing homogeneous system would infringe the patents issuing from this and other applications and therefore be enjoined from operations. The open Grid (or MetaInternet) standards would thus be patent-protected.

As noted earlier, the Internet 3 and WWW (and successors or equivalents) are expected to ensure that any single design standard in widespread use, such as the

Wintel standard (software/hardware) and the Apple MacIntosh standard (also both), are homogeneous as to Grid (or MetaInternet) parallel processing systems as outlined in this application, since the Internet and WWW and equivalents or successors make available such a large pool of homogeneous computers with the same standard, in ever increasingly close proximity as more and more PCs and other devices go online. The increasingly universal connection attribute of the Internet 3 and WWW and successors therefore create virtual homogeneity for most significant brands.

The term homogeneous as it is used here refers to functional design standards primarily, not physical structure, for example, when applied to hardware. In this sense, then, for example, the Intel Pentium II, the Advanced Micro Devices (AMD) K6-6, and the Cyrix MII microprocessor chips are functionally compatible and homogeneous with no need for special emulation software, although they are each structurally quite different and use different microcode at the microchip level. The new Transmeta microprocessors are expected to be functionally compatible and homogeneous through elaborate and highly efficient emulation, potentially an ideal microprocessor for the Grid (or MetaInternet). In contrast, for example, the Apple G3 processor is also structurally different but in addition requires a different operating system and is therefore not functionally compatible and not homogeneous with the Pentium II, K6-6, and MII microprocessors discussed above. Similarly, MS DOS and DR DOS are functionally compatible software PC operating systems and homogeneous, even though their codes are different, whereas Apple MacIntosh operating systems are not functionally compatible or homogeneous with the two DOS systems, except with the addition of special emulation software, which is not efficient. Substantially interchangeable use therefore is a defining element of homogeneity as used in this application. An example of a heterogeneous parallel processing system distributed among many computers, which can be of any sort, is the University of Virginia's Legion system, in contrast to the homogeneous systems discussed above.

This application encompasses all new apparatus and methods required to operate the above described network computer system or systems, including any associated computer or network hardware, software, or firmware (or other component), both apparatus and methods, specifically included, but not limited to (in

their present or future forms, equivalents, or successors): all enabling PC and network software, hardware, and firmware operating systems, user interfaces and application programs; all enabling PC and network hardware design and system architecture, including all PC and other computers, network computers such as servers, microprocessors, nodes, gateways, bridges, routers, switches, and all other components; all enabling financial and legal transactions, arrangements and entities for network providers, PC users, and/or others, including purchase and sale of any items or services on the network or any other interactions or transactions between any such buyers and sellers; and all services by third parties, including to select, procure, set up, implement, integrate, operate and perform maintenance, for any or all parts of the foregoing for PC users, network providers, and/or others.

The combinations of the many elements of the applicant's invention introduced in the preceding figures are shown because those embodiments are considered to be at least among the most useful possible, but many other useful combination embodiments exist but are not shown simply because of the impossibility of showing them all while maintaining a reasonable brevity in an unavoidably long description caused by the inherently highly interconnected nature of the inventions shown herein, which generally can operate all as part of one system or independently.

Therefore, any combination that is not explicitly described above is definitely implicit in the overall invention of this application and, consequently, any part of any of the preceding Figures and/or associated textual description can be combined with any part of any one or more other of the Figures and/or associated textual description of this application to create new and useful improvements over the existing art.

In addition, any unique new part of any of the preceding Figures and/or associated textual description can be considered by itself alone as an individual improvement over the existing art.

The foregoing embodiments meet the overall objectives of this invention as summarized above. However, it will be clearly understood by those skilled in the art that the foregoing description has been made in terms only of the most preferred specific embodiments. Therefore, many other changes and modifications clearly and easily can be made that are also useful improvements and definitely outside the

existing art without departing from the scope of the present invention, indeed which remain within its very broad overall scope, and which invention is to be defined over the existing art by the appended claims.

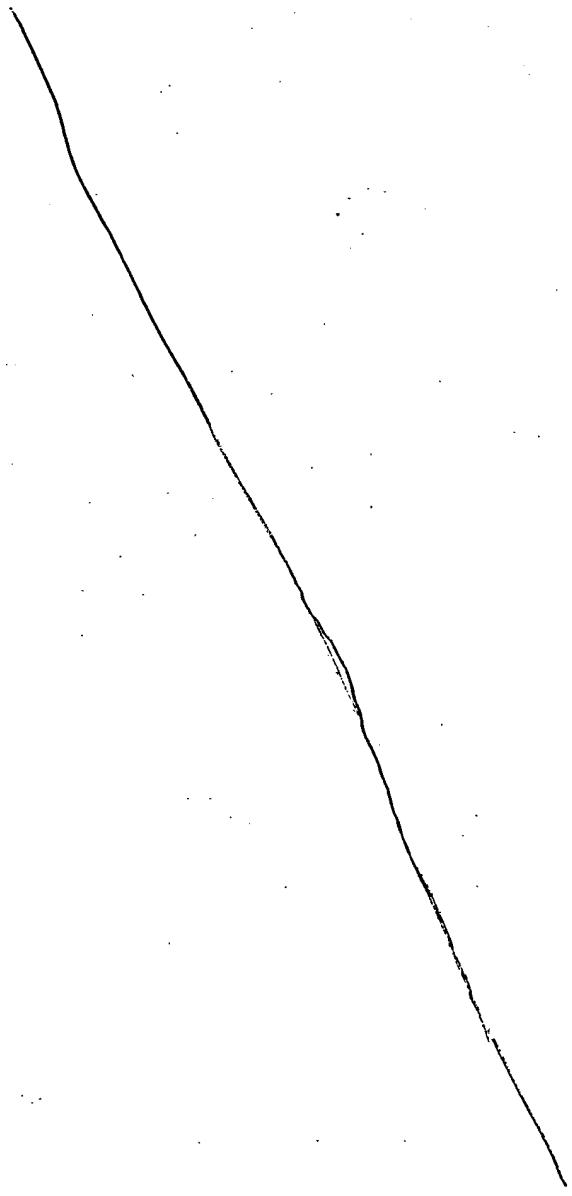


Figure 28 shows a silicon wafer 500 used to make microchips. The largest wafers 500 in current use are 300 mm (12inches) in diameter and can contain as many as 13 billion transistors. Current state of the art in microchip fabrication is 0.13 micron process technology and the next process will be measured in nanometers (90 nm). As shown in Figure 28, microchips 501 are separated by an edge portion 502. A microchip 501 can be a PC 90 microchip.

Figure 29A shows a microchip 501 surrounded by adjoining portions of adjoining microchips 501 in a section of the silicon wafer 500. The microchip 501 is bounded by edge portions 502. Although the current state of the art in microchip fabrication on a silicon wafer is to use only one process on a wafer, it is the applicant's invention to use two or more fabrication processes on a single silicon wafer 500.

As shown in the example shown in Figure 29A, one process can be located on one section 511 of the microchip 501, while a second process can be located on a second section 521 of the microchip 501. As shown in the example of Figure 29A, a third process can be located on a third section 531 of the microchip 501; additional processes can also be located on other sections of the microchip 501.

The processes can be completely separate while at least sharing the common silicon wafer 500 base and the processes can occur at different fabrication facilities, including those

owned by different manufacturers. Alternatively, two or more separate processes may have common sub-processes that can be integrated, which is to say done at the same time. Sections of the microchip 501 that are not undergoing a process can be protected from that process by a protective coating that is unaffected by that process and removed after that process. There can be one or more temporary protective coatings, which can remain on for more than one process.

The separate sections of the separate fabrication processes of the microchip 501 can be in any shape or pattern on the microchip. As shown in the Figure 29A example, one or more separate processes can be located on adjoining portions of adjoining microchips. For example, as shown in Figure 29A, section 521 is located on the lower portion of one row of microchips 501 and on the upper portion of the adjoining row of microchips 501, which would be positioned upside down on the wafer 500, so that the contiguous area of the section 521 process is maximized. Similarly, section 531 is shown in the example located on the lower portion of the adjoining row of microchips 501 and on the upper portion of the middle row of microchips 501. Alternatively, all of the microchips 501 of the wafer 500 can be positioned upright on the wafer.

The applicant's invention includes any fabrication process on a silicon wafer 500 and can include wafers made of other materials suitable for microelectronic devices, such as

gallium arsenide. The fabrication processes in current widespread use are generally CMOS (complementary metal-oxide semiconductor), but can be bipolar or other. The separate processes (and separate sections 511, 521, and 531 shown in Figure 29A) can be for general purpose microprocessor (including one or more cores), memory (DRAM or non-volatile like Flash or MRAM or ovonic), analog (including radio and/or laser), digital signal processing (DSP), micro-electromechanical system (MEMS), field programable gate arrays (FPGA), graphic processing unit (GPU), microprocessor chipset, and others.

The applicant's invention facilitates a"system of a chip" (SoC), such as the earlier described PC 90 microchip, by allowing most or all of the micro components of a PC to be located on a single microchip. Even the consolidation of only two microchips into a single microchip provides a significant increase in processing speed and reduced power consumption. The silicon die becomes the motherboard for all the micro components of the PC, leaving only the macro components like battery, power supply, and input/output (I/O) connections to be located on the printed circuit motherboard. The result is ultra-large-scale-integration.

Figure 29B shows the microchip 501 embodiment of Figure 29A after the die has been separated from the silicon wafer 500 and positioned in a microchip package 503. Both Figures 29A and 29B are topviews.

The fabrication processes illustrated in Figures 29A-B can include material like silicon germanium, gallium arsenide, indium phosphide and others used, for example, as deposits on silicon. Besides using different materials in different sections of the microchip, different size processes can be used in different microchip sections, such as a 0.13 micron process on section 511 and a 0.18 micron process on section 521 in the Figure 29A example. All or parts of the microchip 501 can be synchronous or asynchronous. Both different size and different material processes can be combined on different sections of the microchip 501.

Although the maximum increase in speed and decrease in power consumption can be achieved by putting all micro or nano components on a single "system on a chip", such as for a PC, even a minimal combination of just two different micro or nano components on a single microchip 501 can yield a very significant increase in speed and decrease in power consumption. To take a very simple example, a silicon wafer 500 can have 256MB of DRAM manufactured onto a section 531 of the microchips 502 located on the wafer by one factory; when that DRAM process is completed, a second factory can add a general purpose CPU like a Pentium 4 to a second section 511 of the microchips 501 on the silicon wafer 500. Such an approach allows direct communication between microprocessor and DRAM on the microchip 501 for much greater speed and reduced power.

Since 256MB DRAM is an inexpensive commodity product currently, especially if purchased as wafers 500, there would be little or no increase in the production time of the microprocessor.

Figure 30A illustrates the applicant's invention, which is an alternative method of uniting separate fabrication processes on the same microchip 501. Sections 501^1, 501^2, and 501^3 of Figure 30A correspond to sections 511, 521, and 531 of Figures 29A & 29B in that both sets of sections represent three separate processes, but in Figure 30A each section is a separate die cut from a wafer 500 and all three sections are united in a single package 50s. The section dies 501^1, 501^2, and 501^3 can be held together by the chip package 503 or can be gluedtogether or a combination of the two in parts or the whole; in addition, the section dies can be assembled into a chip package 503 or the package can be assembled around the dies or a combination of both partially or completely.

The separate process dies illustrated in the Figure 30A example are preferably assembled with the surface that the process is on in each die being substantially level with each other, so that both process surfaces of the dies form a plane that is substantially flat. The edges of the dies are configured so adjoining dies fit together as closely as possible, as shown in Figure 30A at 502^2 and 502^3.

The circuits of dies 501^1, 501^2, and 501^3 are connected

at their edges 502^3 and 502^2 by interconnect lines 580 that can be widened as shown in 581 of Figure 30B, which shows a portion of die edge 502^3 or 502^2 in an enlargedview. A process can be added in the area 591 overlapping the edges of the dies at 502^3 and 502^2 bounded by lines 590; in that process interconnect lines 580 of the two separate dies can be connected by laying down connection at 582 that connect to the elarged portions 581 of the interconnect lines 580, as illustrated in Figure 30B.

Figure 30C shows that the die edges 502^3 and 502^2 can have any shape or pattern, not just a straight line shown above in Figures 30A &30B.

Figure 31 shows a combination of the applicant's methods shown in Figures 29 and 30. Microchip 501 as shown in Figure 29 is shown assembled with separate dies 501^1, 501^2, and 501^3 into a microchip package 503, with edges between dies at 502^1, 502^2, 502^3, and 502^{23}, which could include a connection process such as the example shown in Figure 30B.

The microchip 501 dies shown in Figures 29-31 can be packaged using FCPGA (flip-chip pin grid array), FCBGA (flip-chip ball grid array), BBUL (bumpless build-up layer) or other technology.

Any of the embodiments shown in Figures 28, 29A-29B, 30A-30C, and 31 can be combined with one or more other embodiments shown in thos figures or in the preceding Figures 1-27 and descibed herein.

Fig. 1

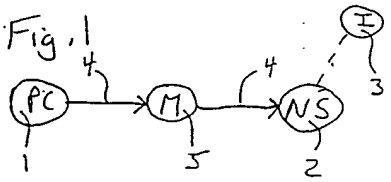


Fig. 2

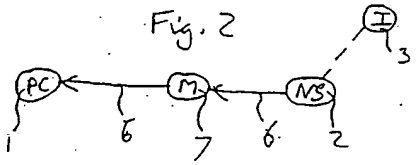


Fig. 3

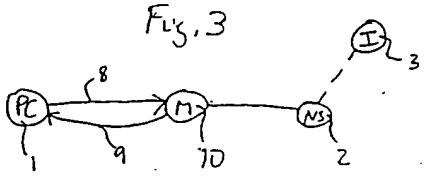


Fig. 4A

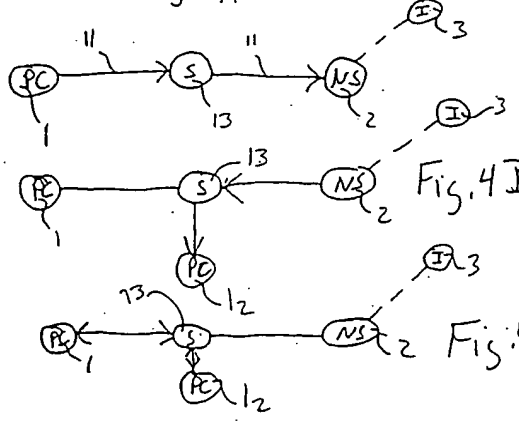


Fig. 4B

Fig. 4C

Fig. 5A

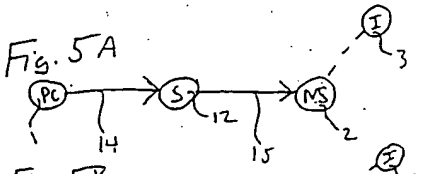


Fig. 5B

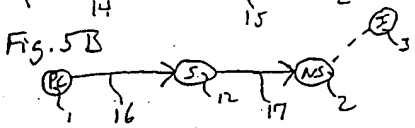


Fig. 6

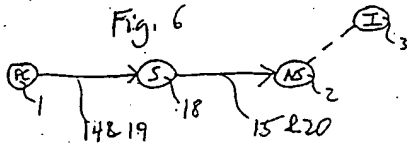


Fig. 7

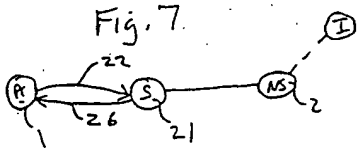


Fig. 8

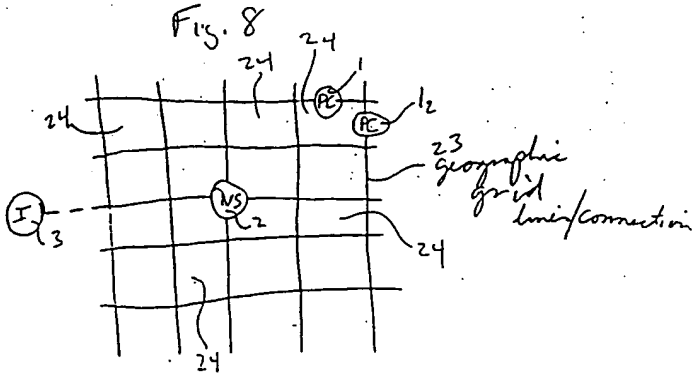


Fig. 10B

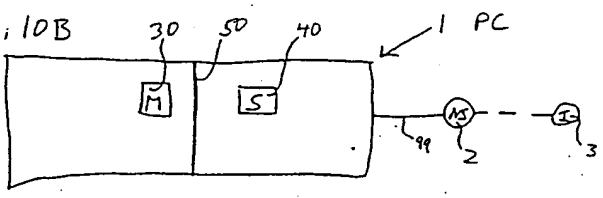


Fig. 10A

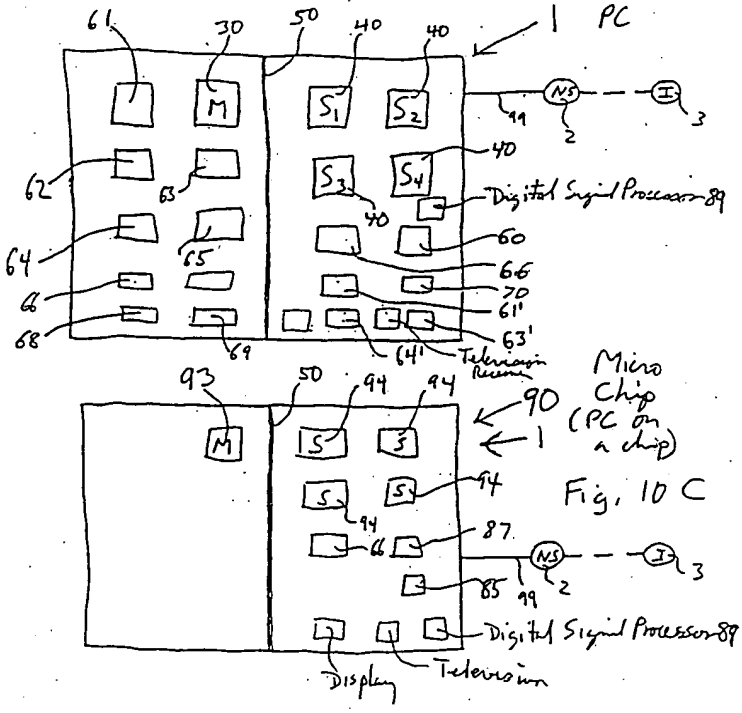


Fig. 10C

Fig. 9

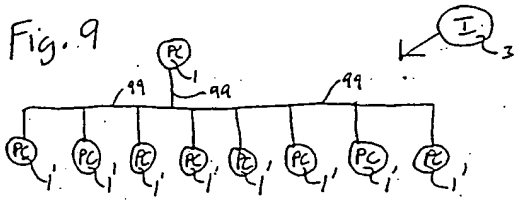


Fig. 10D

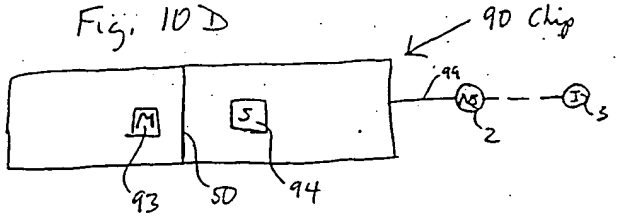


Fig. 11

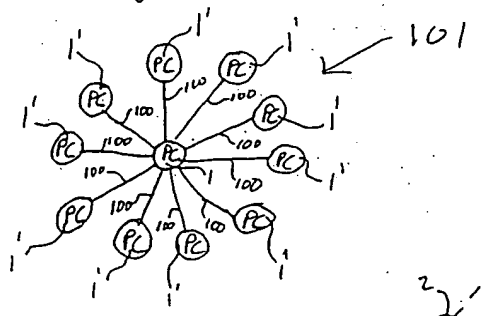


Fig. 10I

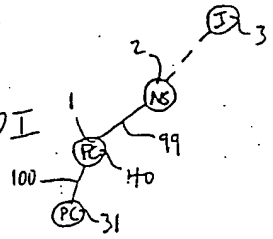


Fig. 10E

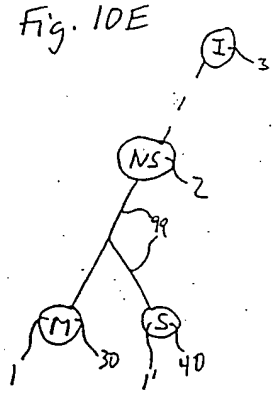


Fig. 10F

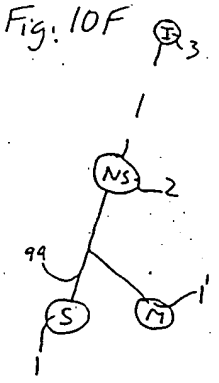


Fig. 10G

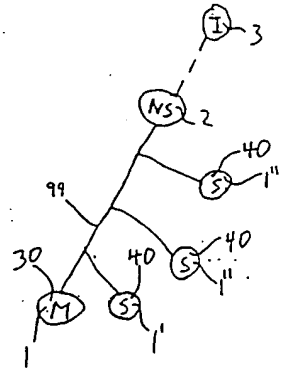


Fig. 10H

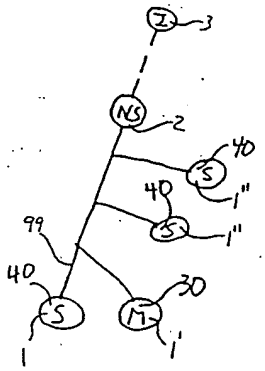


Fig. 12

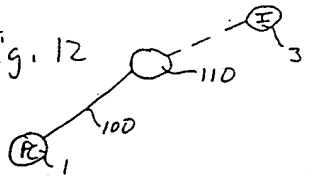


Fig. 13

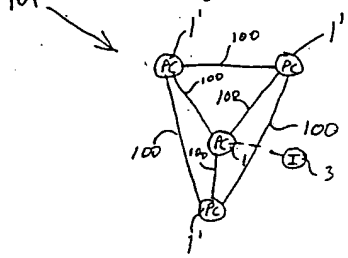


Fig. 14A

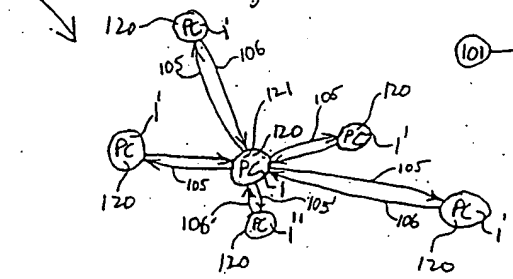


Fig. 14B

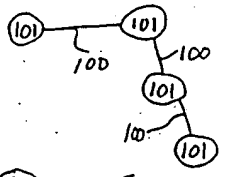


Fig. 14C

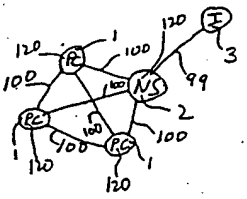


Fig. 14D

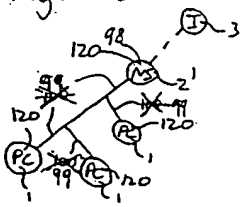


Fig. 15

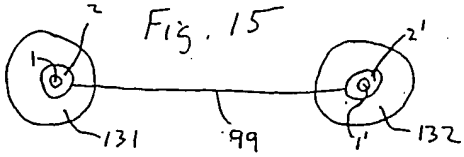


Fig. 10K

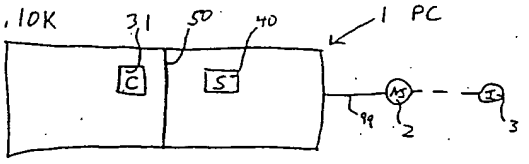
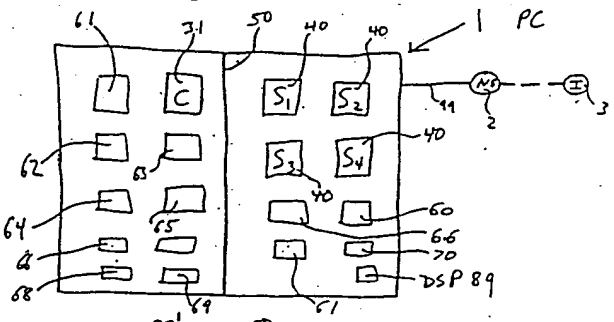


Fig. 10J



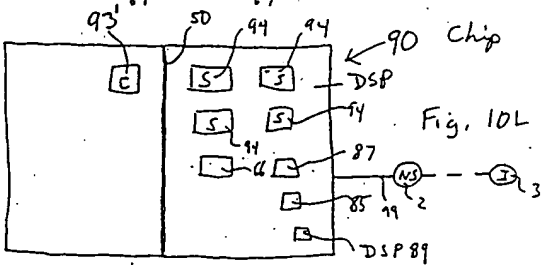


Fig. 10L

Fig. 10M

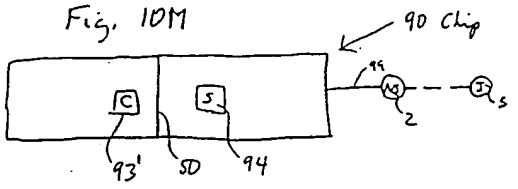


Fig. 10"O"

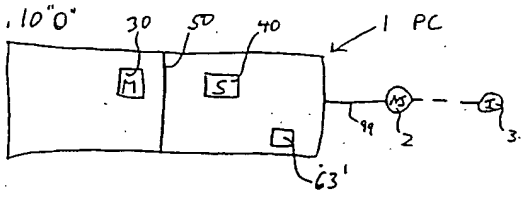
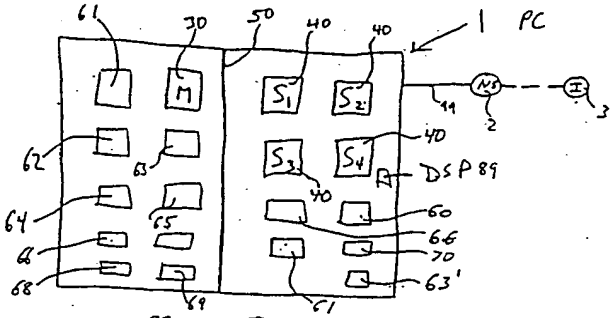


Fig. 10N



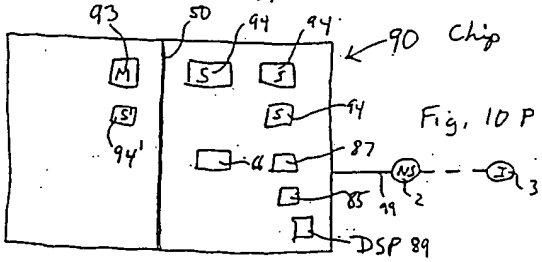


Fig. 10P

Fig. 10Q

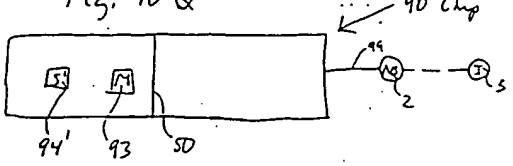


Fig. 16A

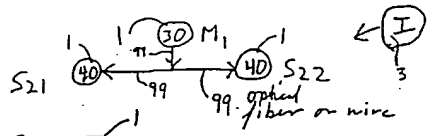


Fig. 16B

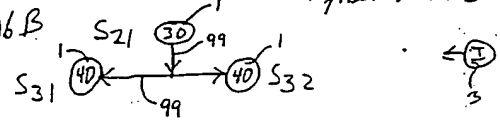


Fig. 16C

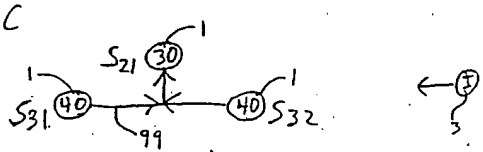


Fig. 16D

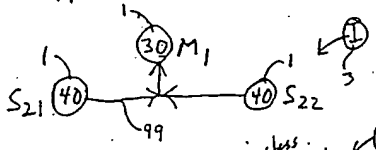


Fig. 16G

Fig. 16H

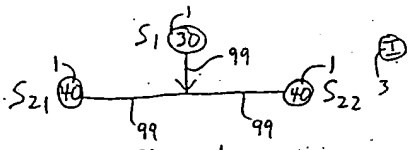


Fig. 16I

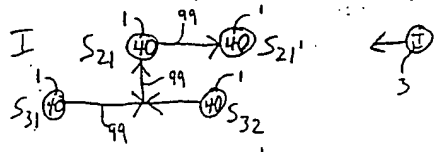


Fig. 16J

Fig. 16 E

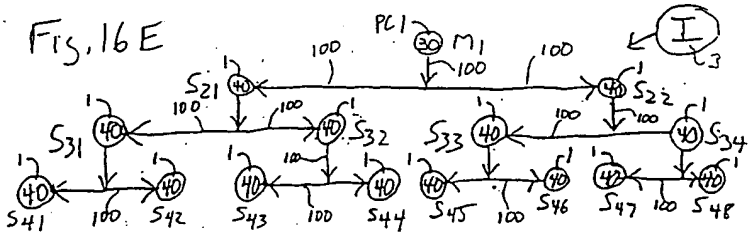


Fig. 16 F

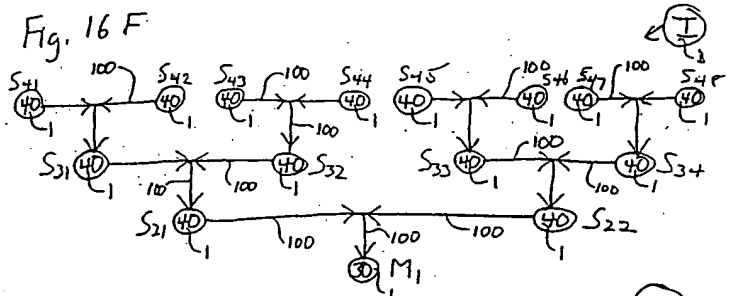


Fig. 16 K

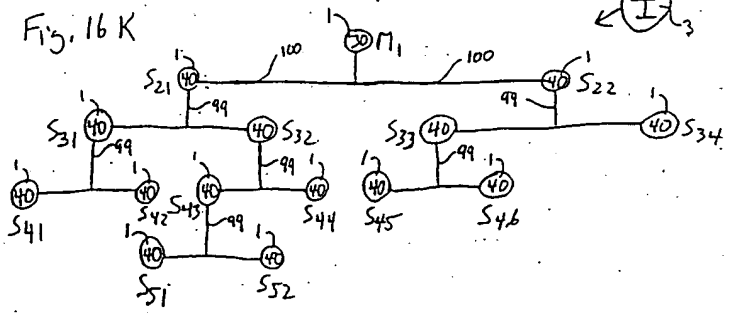


Fig. 16L

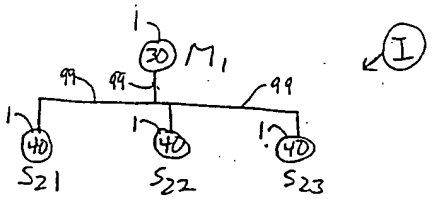


Fig. 16M

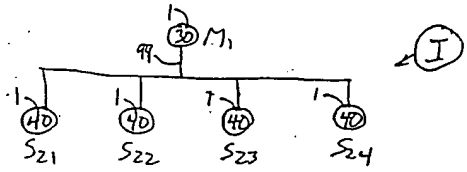


Fig. 16N

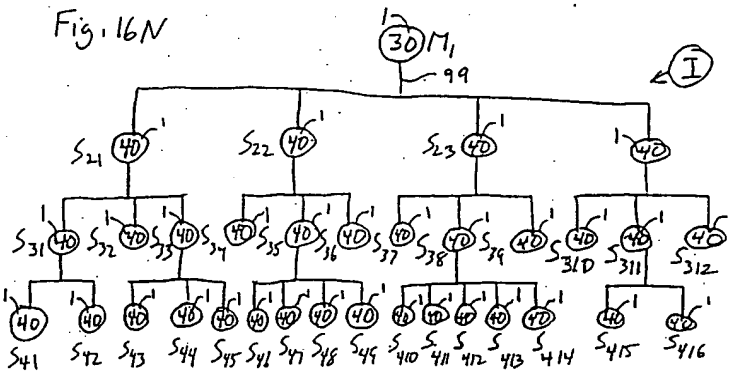


Fig. 16O

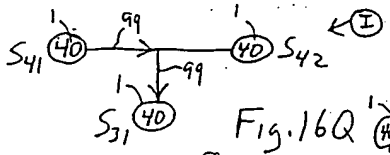


Fig. 16Q

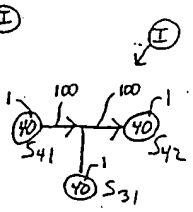


Fig. 16P

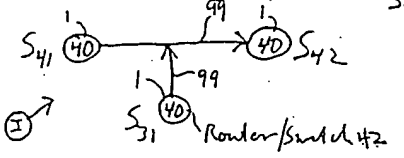


Fig. 16X

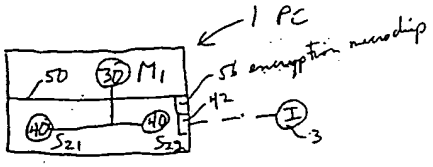


Fig. 16Y

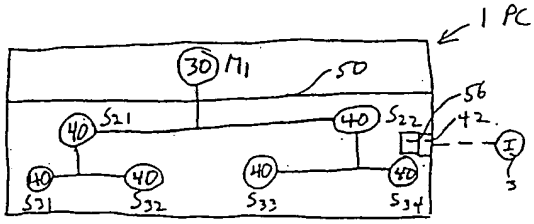


Fig. 16Z

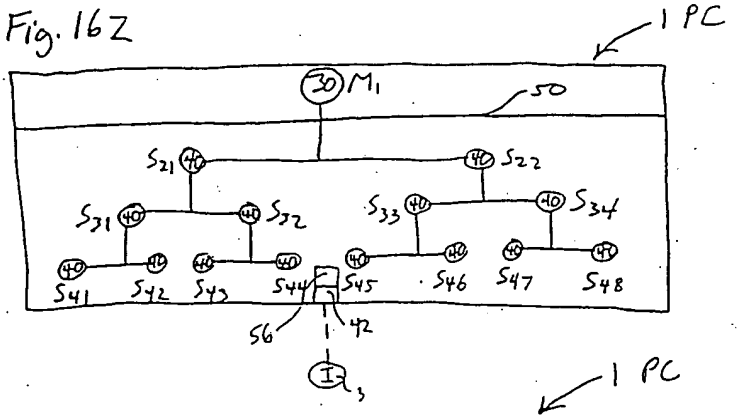


Fig. 16AA

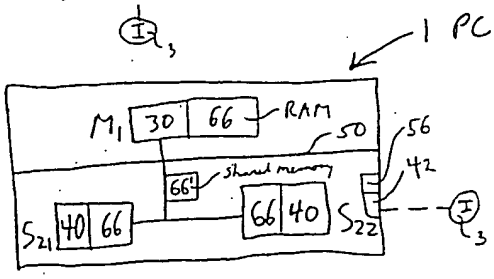


Fig. 16R

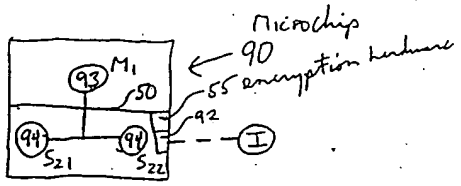


Fig. 16S

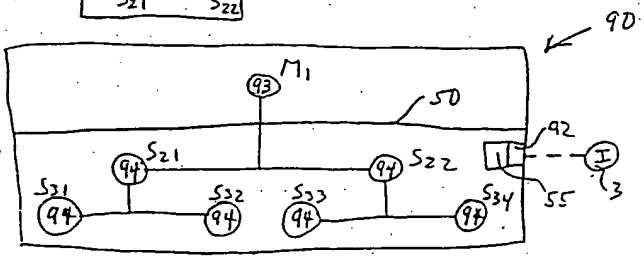


Fig. 16T

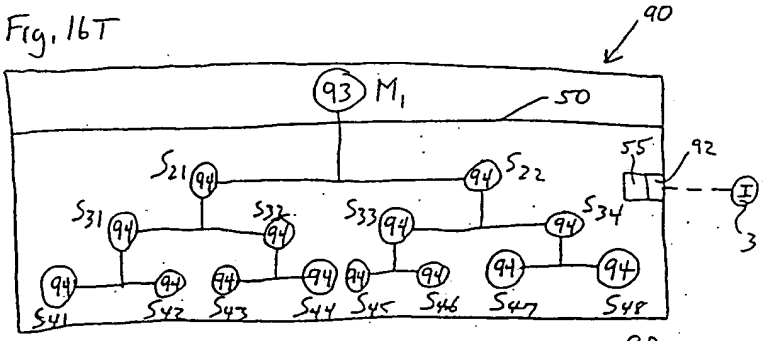


Fig. 16U

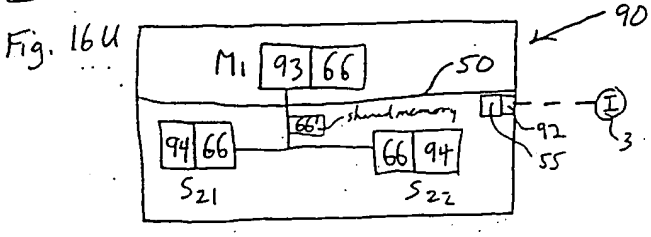


Fig. 16V

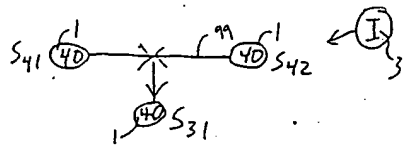


Fig. 16W

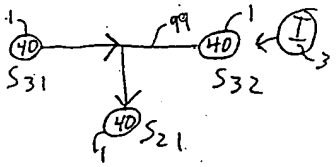


Fig. 17C

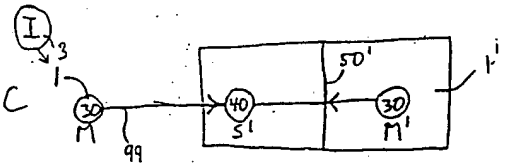


Fig. 17A

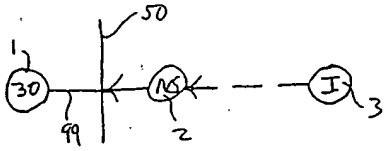


Fig 17B

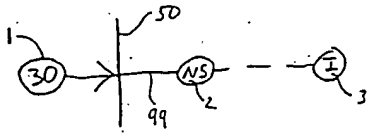


Fig. 17D

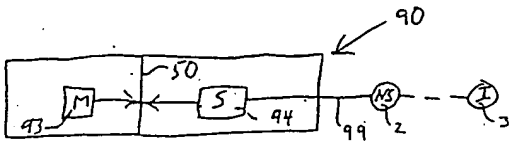


Fig. 18A

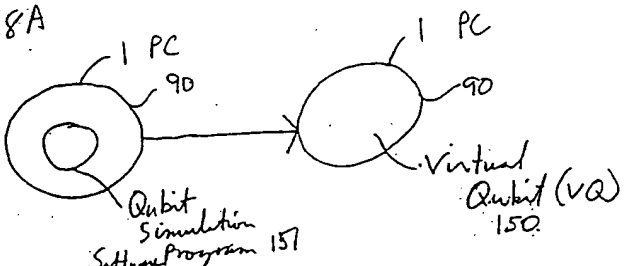


Fig. 18B

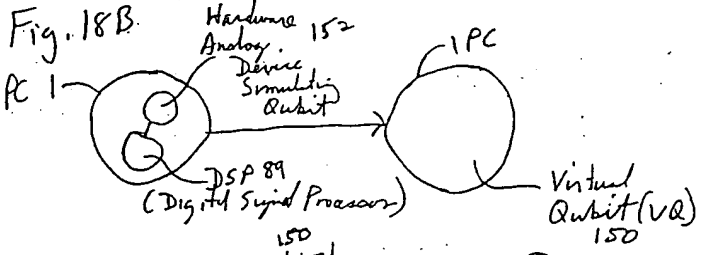


Fig. 18C

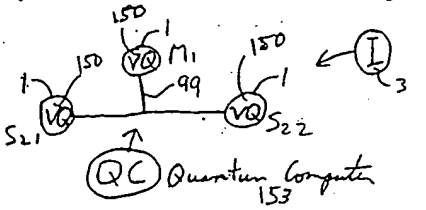


Fig. 18D

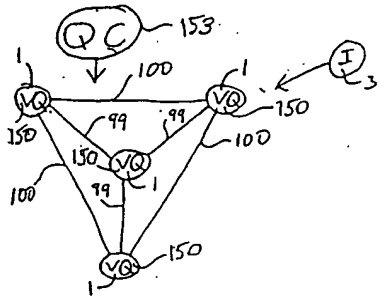


Fig. 19

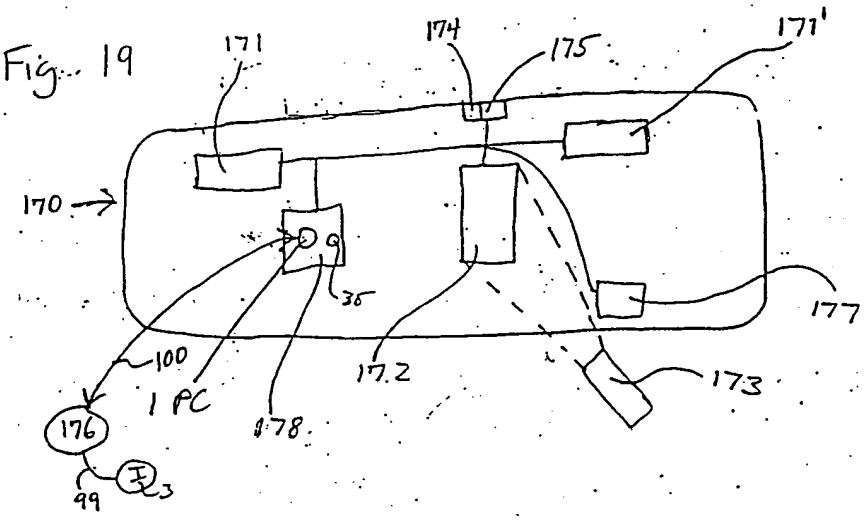


Fig. 16 A B

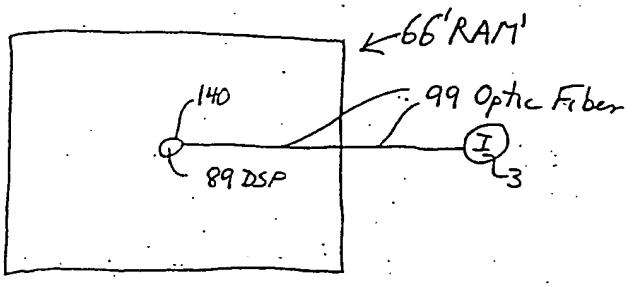


Fig. 21C

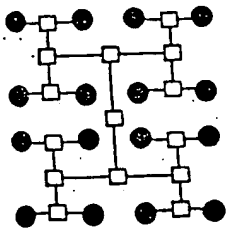


Fig. 20A

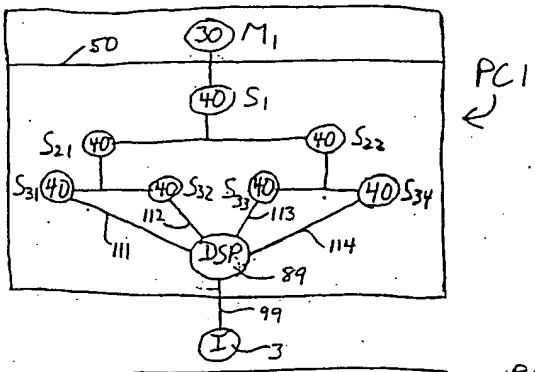


Fig. 20B

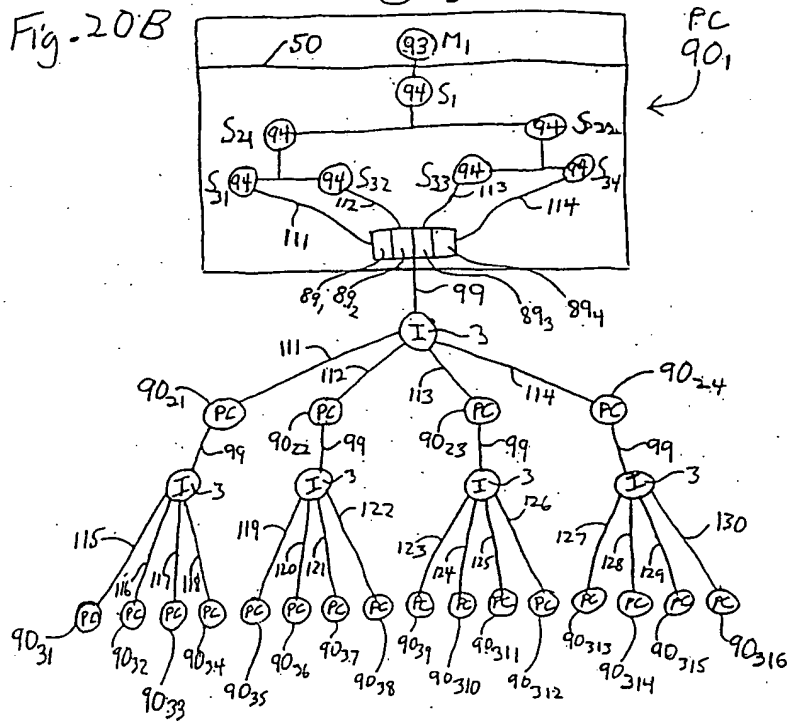


Fig. 21A

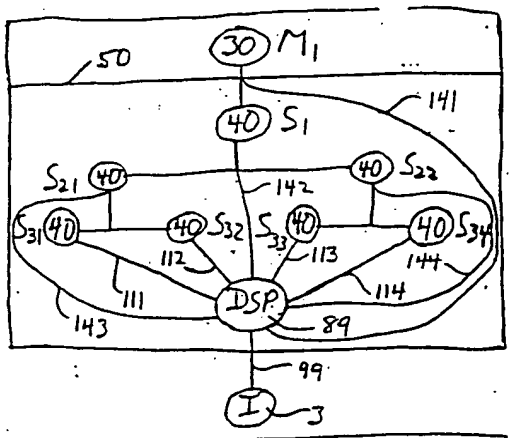


Fig. 21B

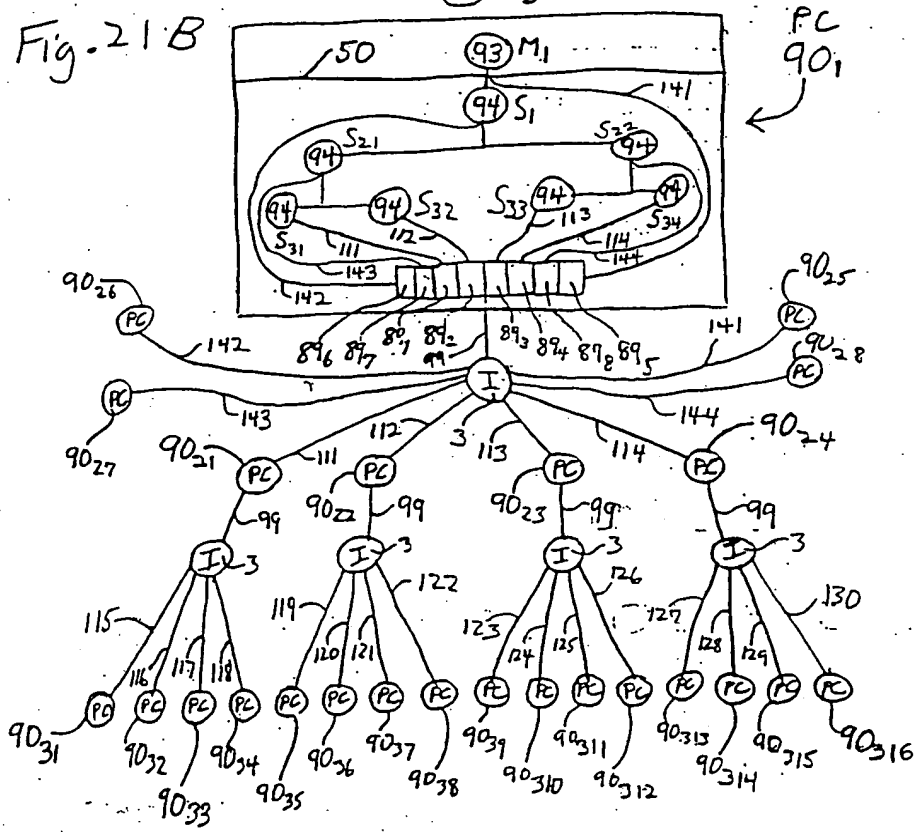


Fig. 22A

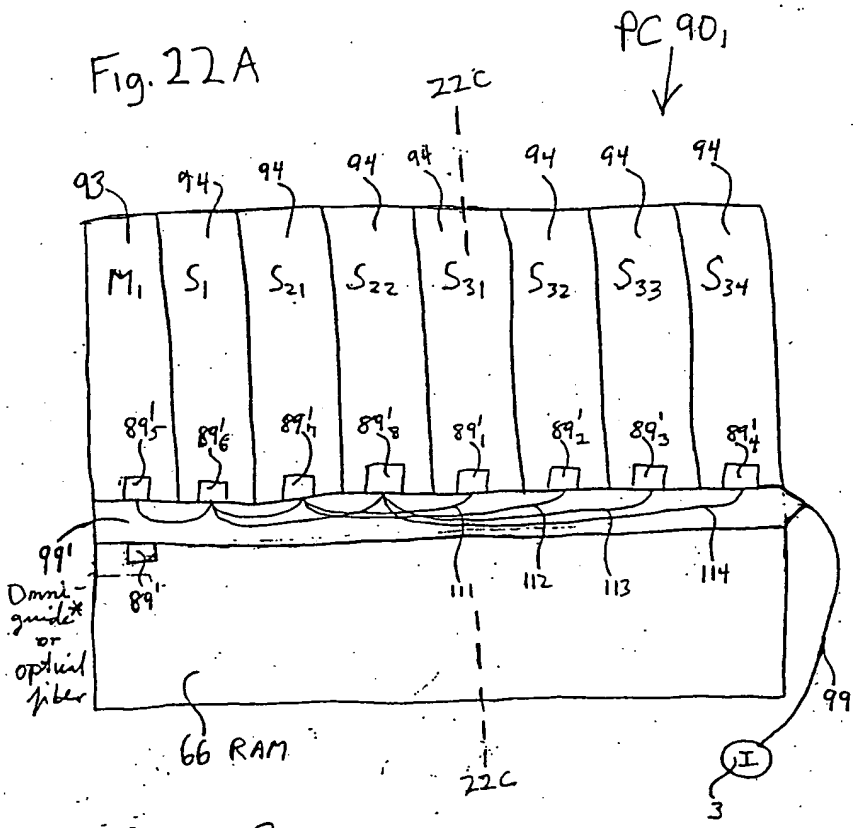


FIG. 22B

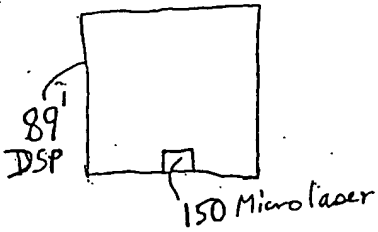


FIG. 22C

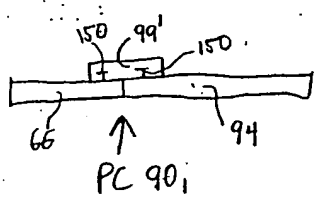


Fig. 23A

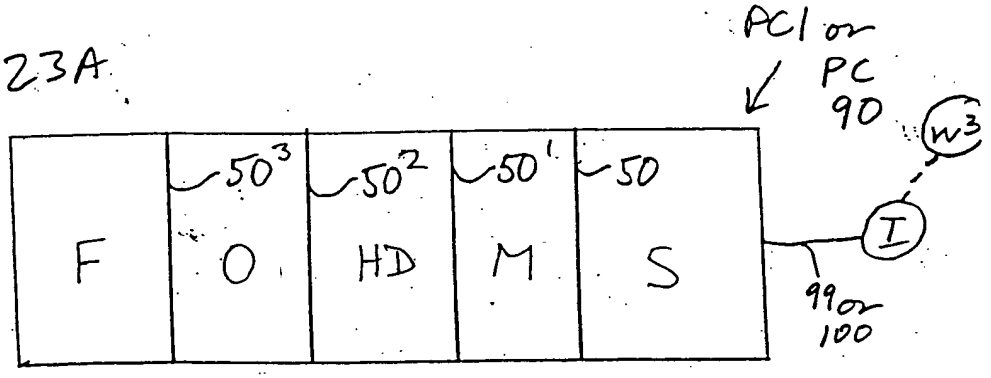


Fig. 23B

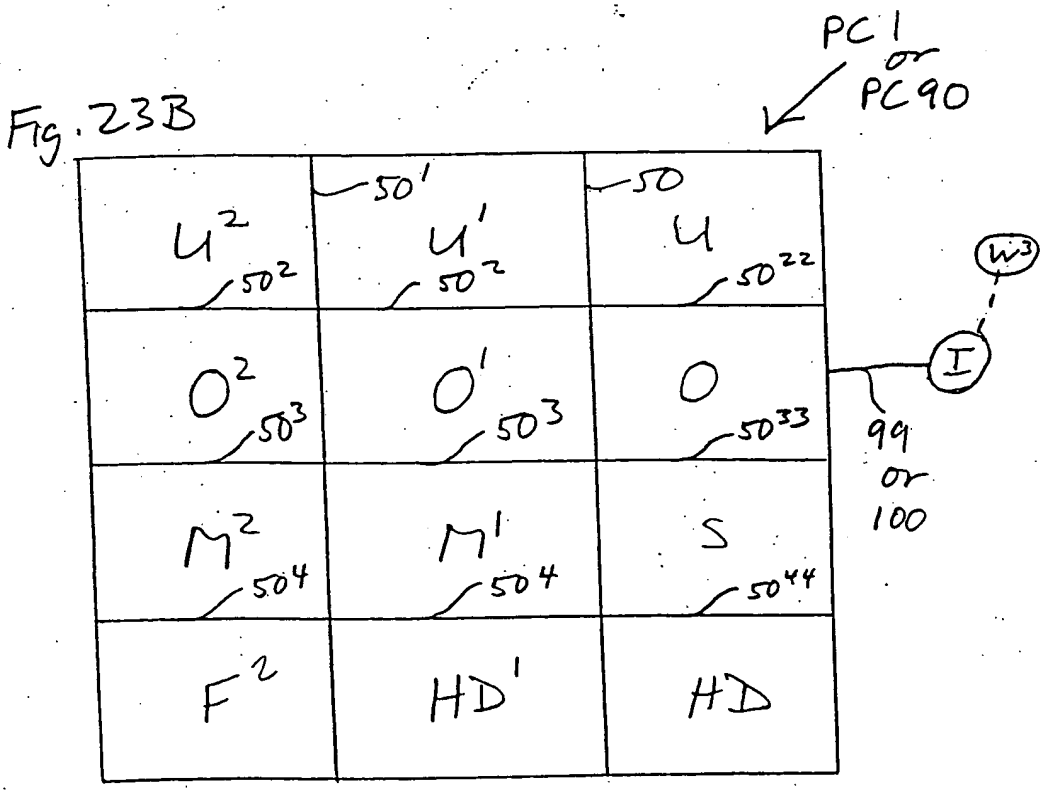
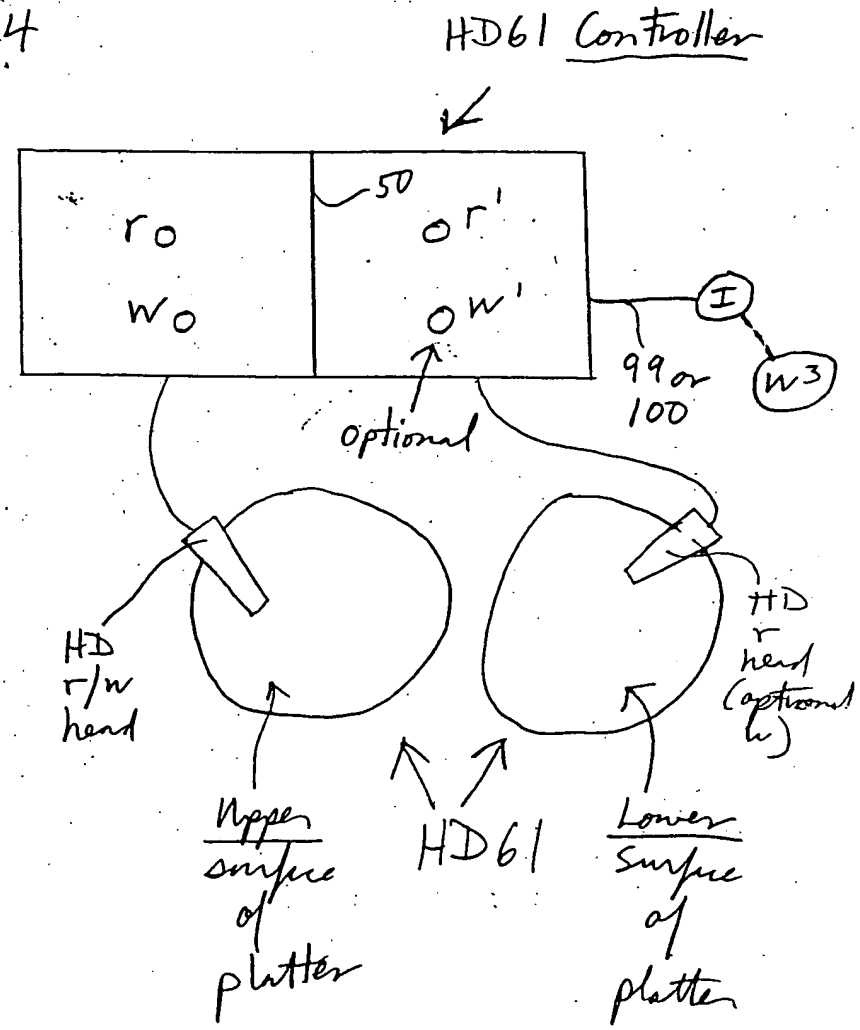


Fig. 24


HD61 Controller
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r0
w0
or'
ow'
I
99 or 100
W3
optional
HD r/w head
HD r head (optional w)
Upper surface of platter
HD61
Lower surface of platter

Fig. 23C

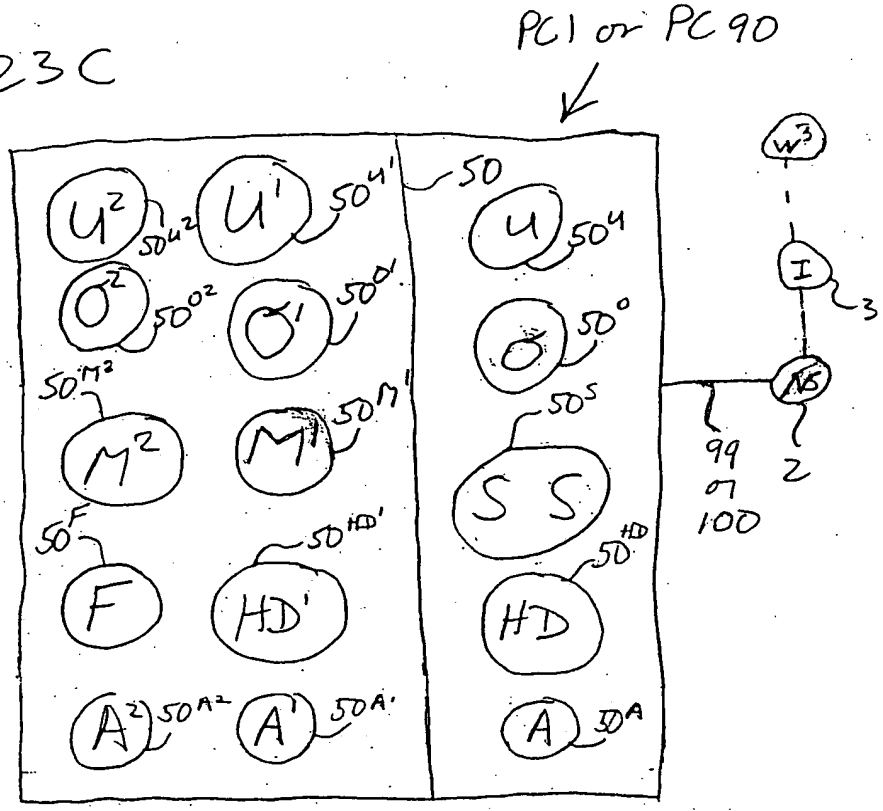

Fig. 23D

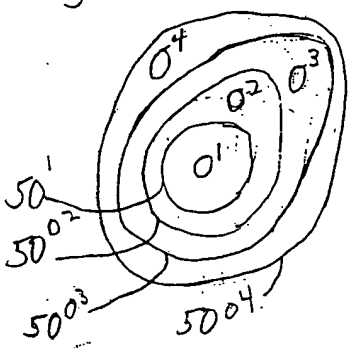

Figure 23E

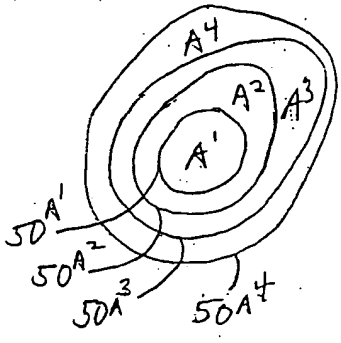

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Fig. 25A

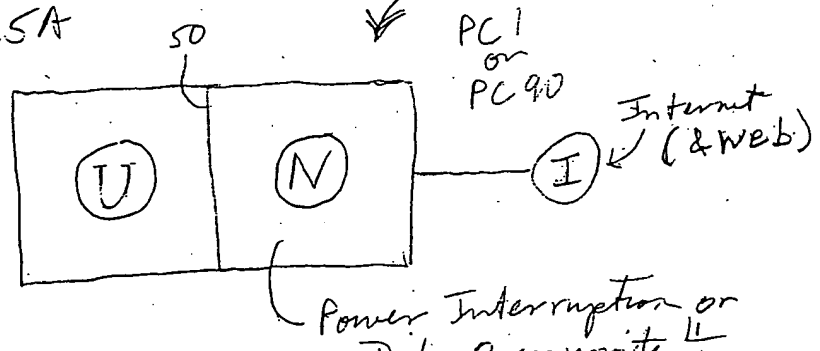

Fig. 25B

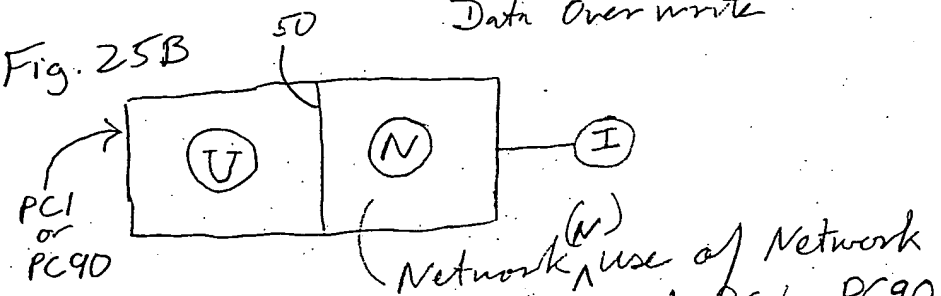

Fig. 25C

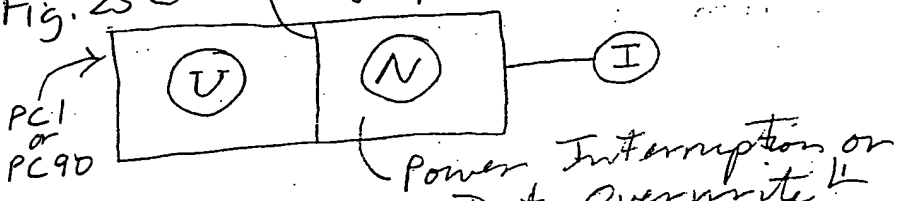

Fig. 25D

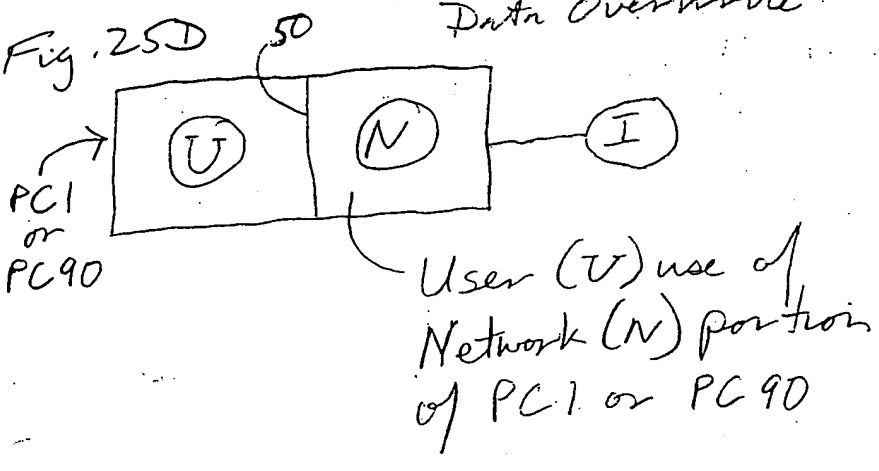

Fig. 26A

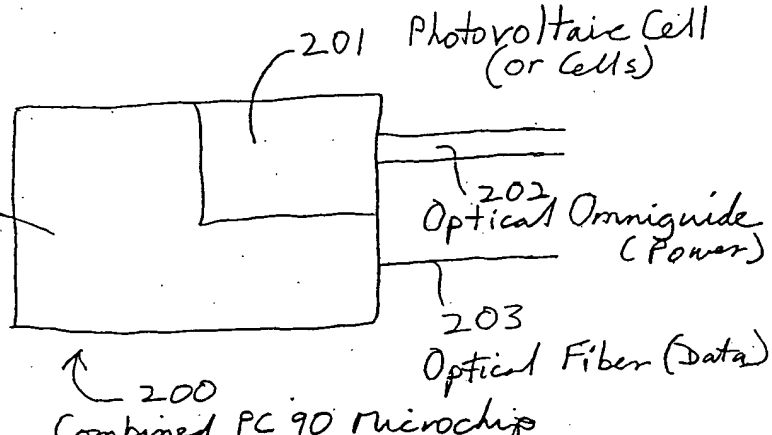

Fig. 26B

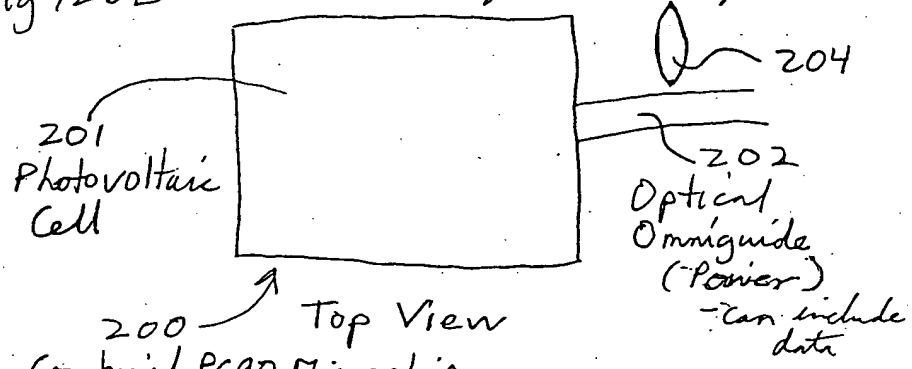

Fig. 26C

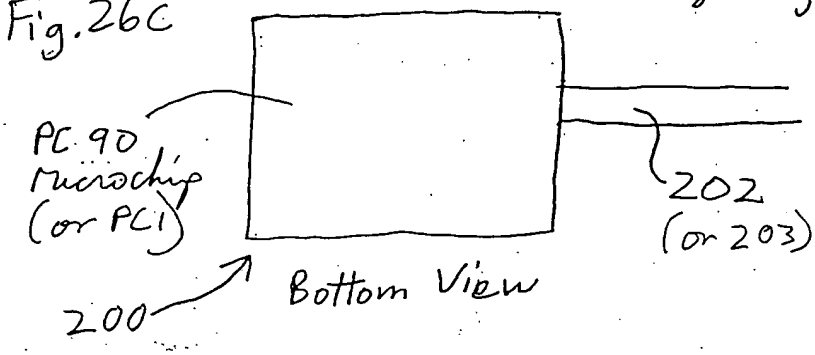

Fig. 27A

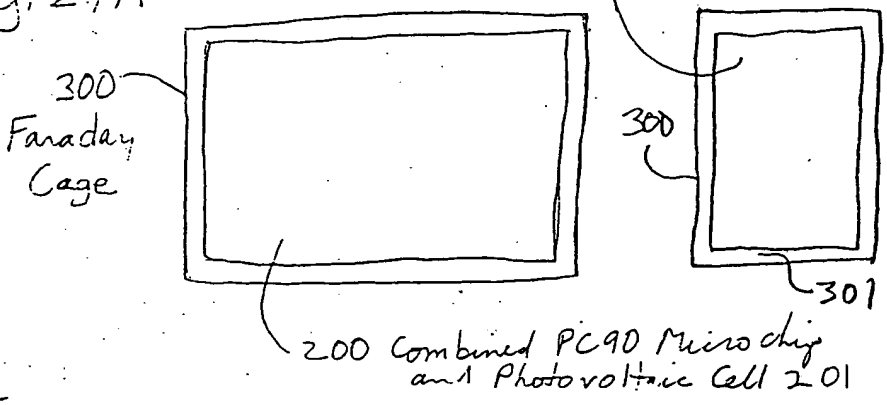

Fig. 27G

Fig. 27B

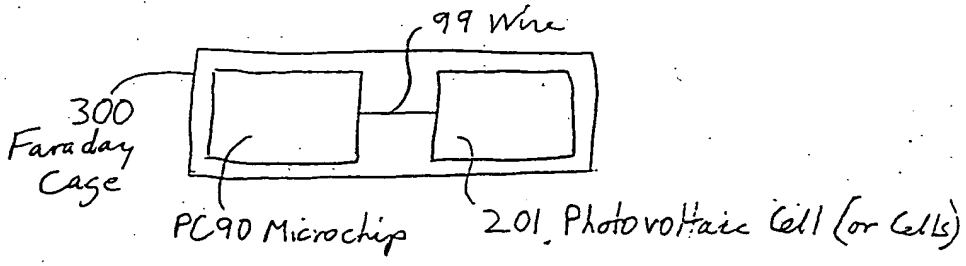

Fig. 27C

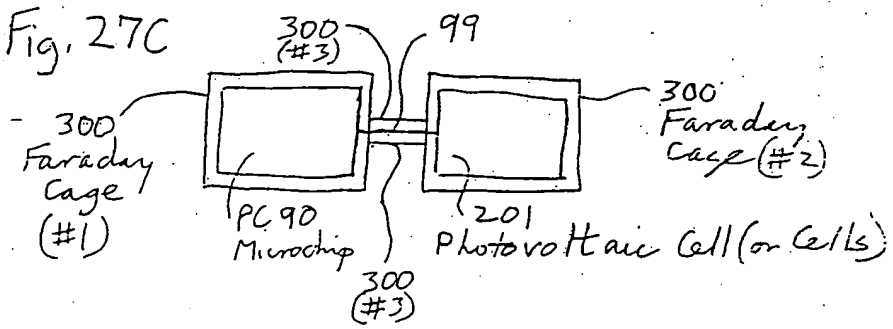

Fig. 27D

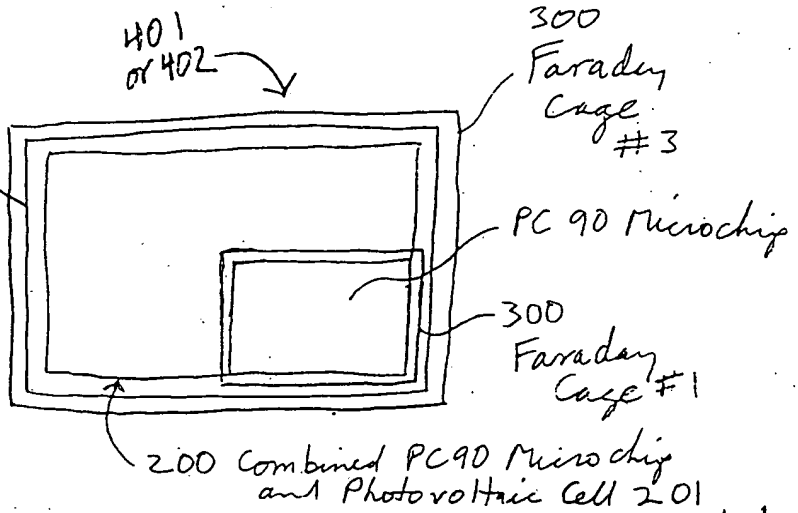

Fig. 27E

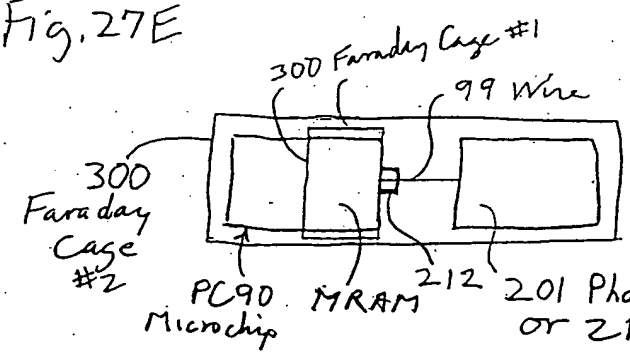

Fig. 27H

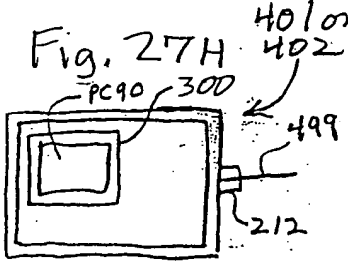

Fig. 27F

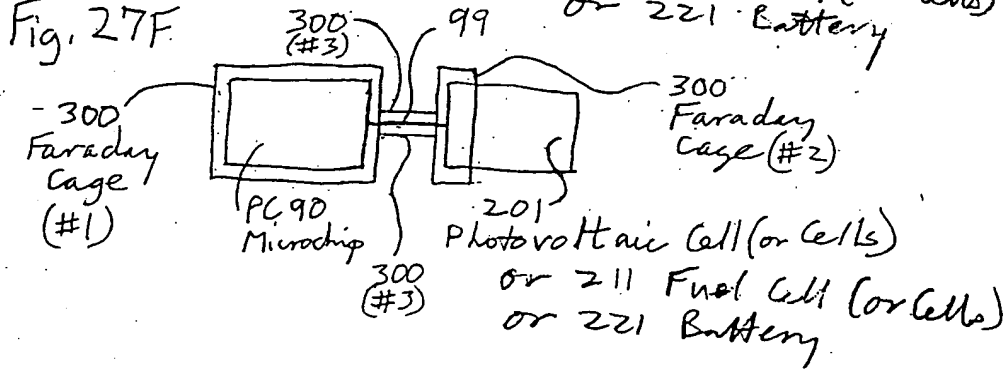

Fig. 28

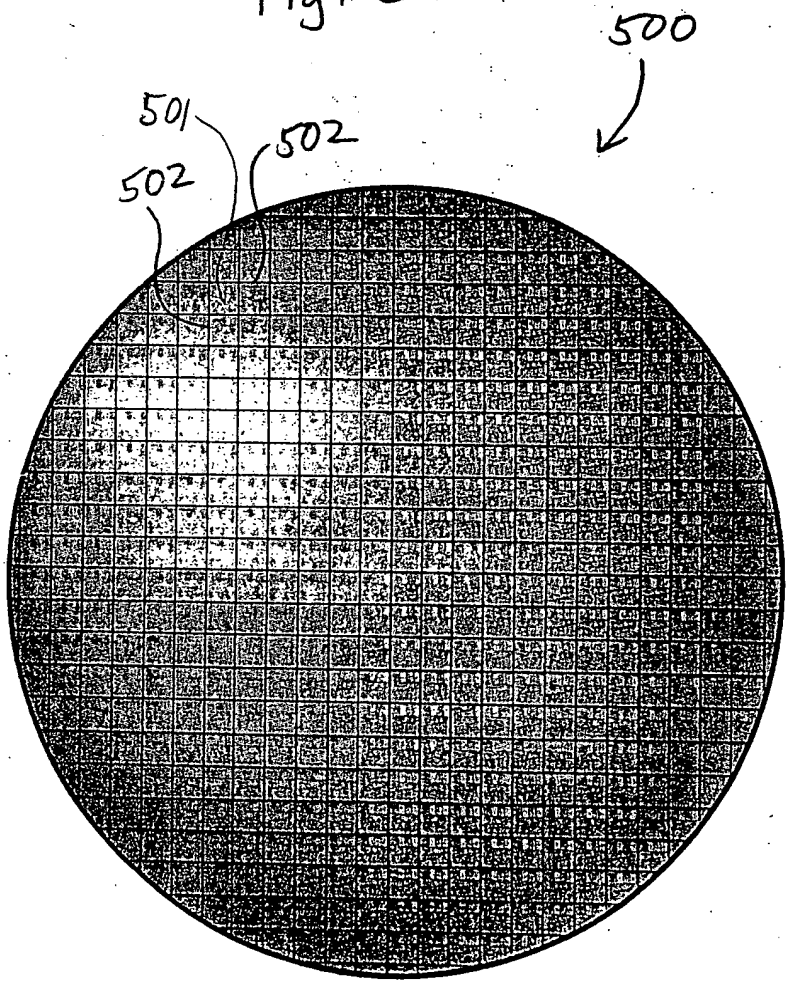

Fig. 29A

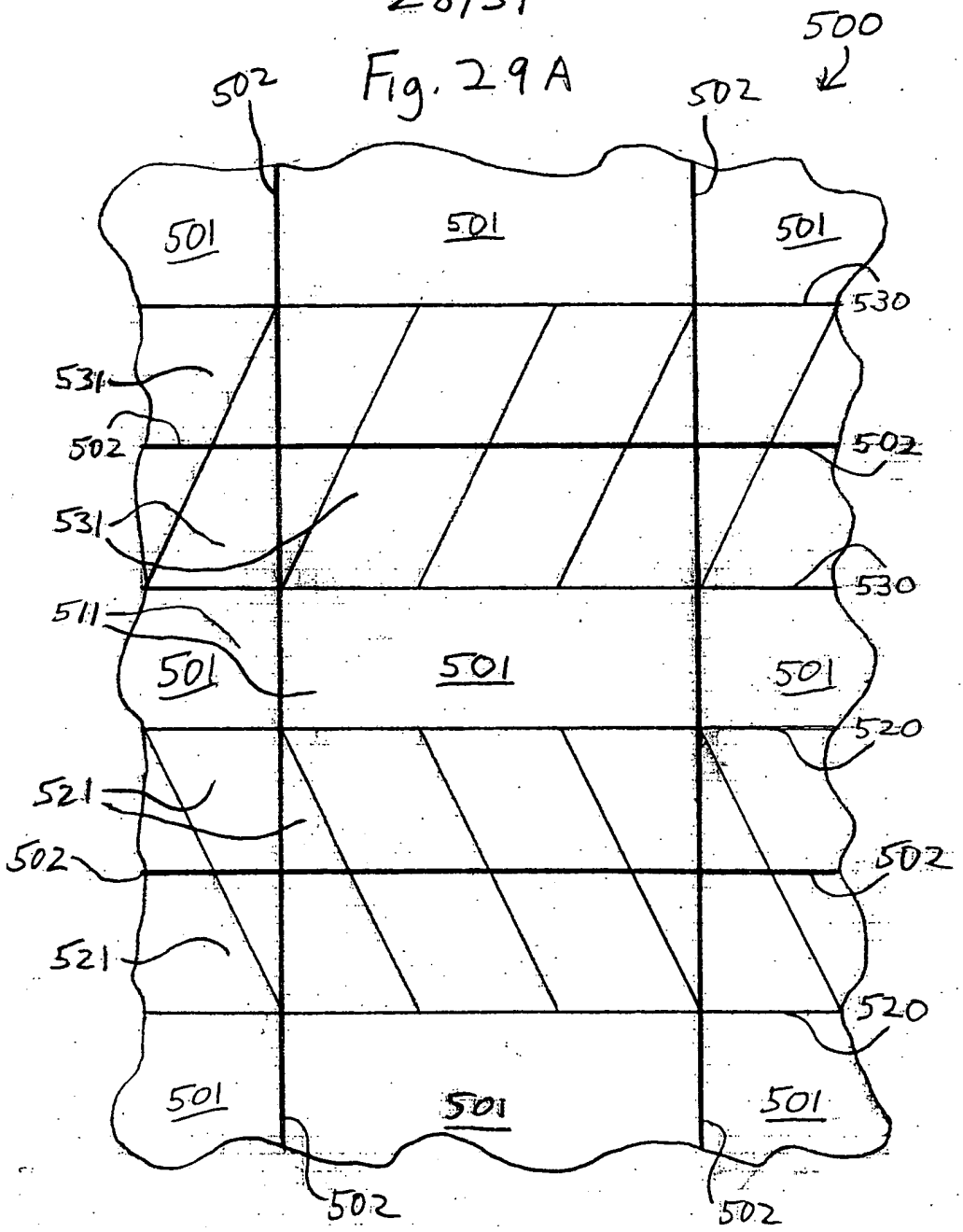
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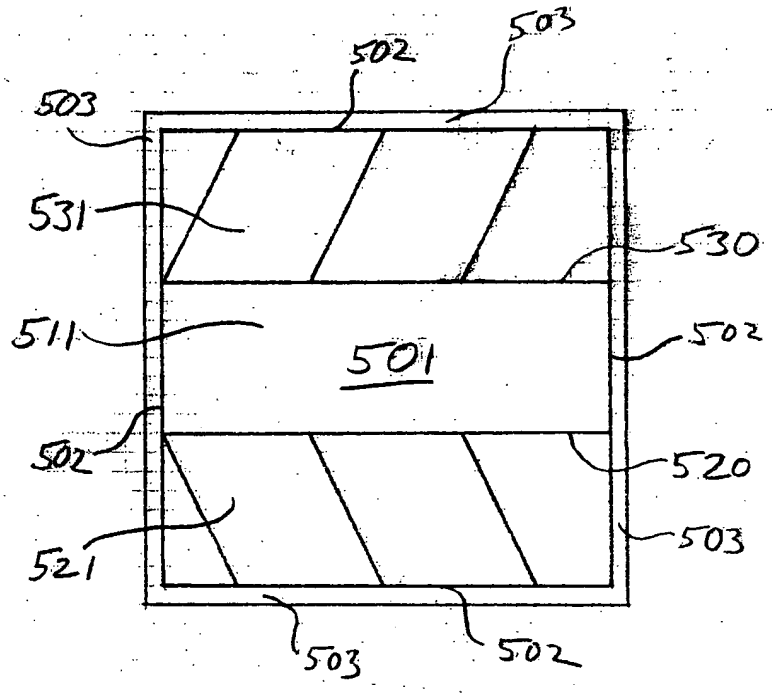
Fig. 29B



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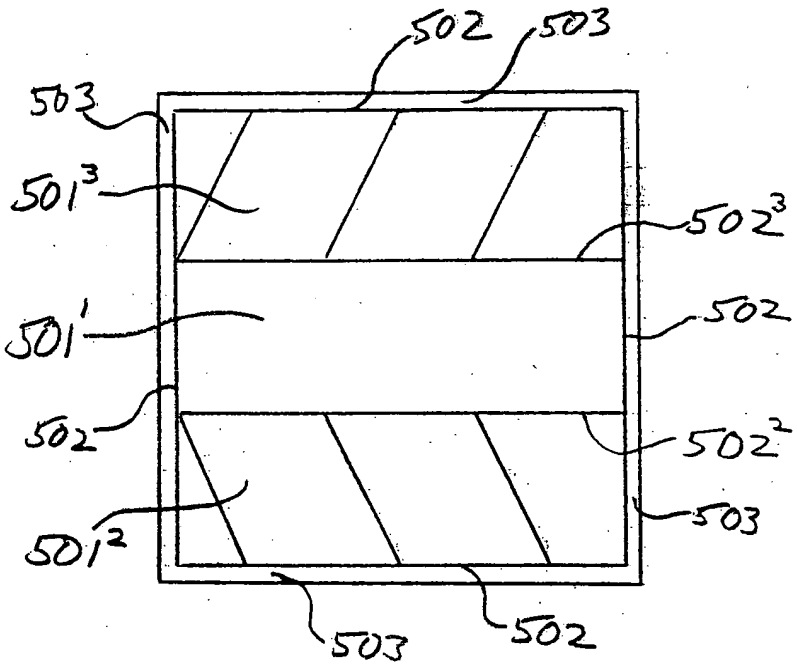


Fig. 30B

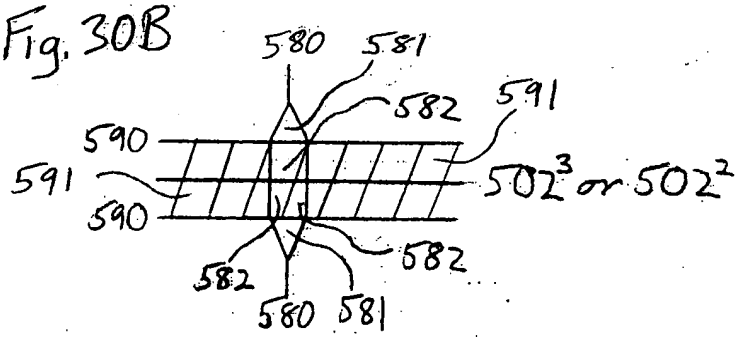
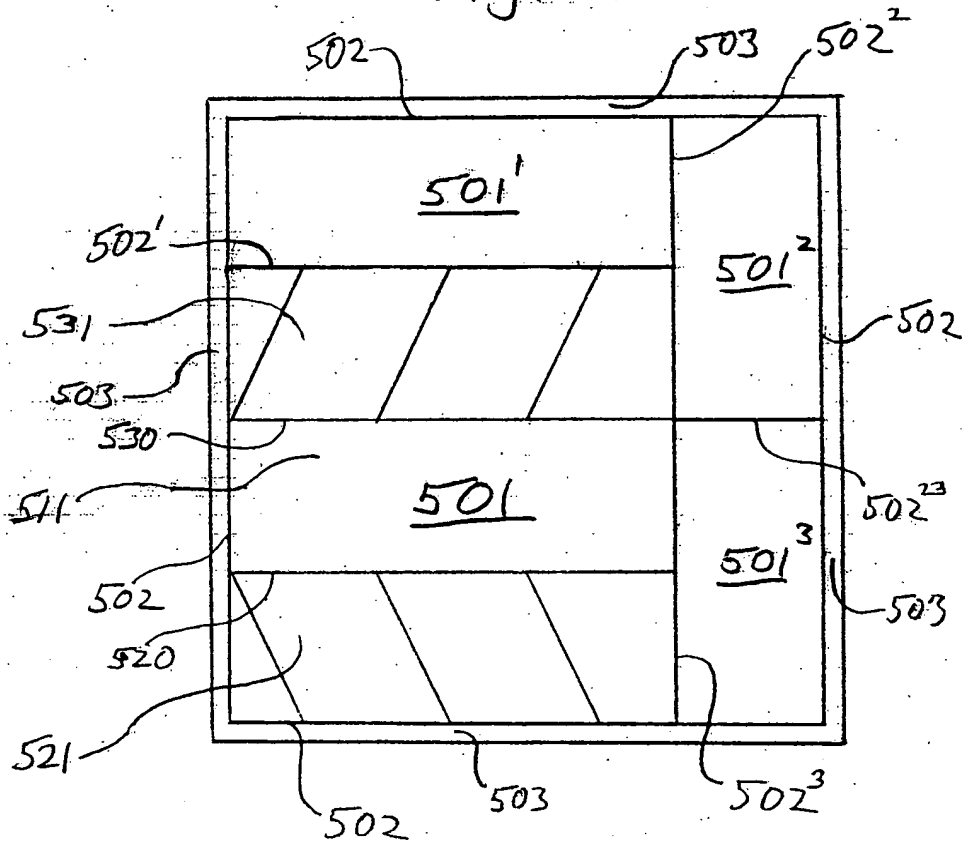


Fig. 30C

Fig. 31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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re PATENT APPLICATION of
Inventor(s): FRAMPTON E. ELLIS

Appln. No.: 60/418,177

Group Art Unit:

Filed: October 15, 2002

Examiner:

Title: GLOBAL NETWORK COMPUTERS

Date: October 24, 2003

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Alexandria, VA 22313-1450

Sir:

It is respectfully requested that Sharon Knott

be allowed to inspect and make copies of any and all documents in the Patent and Trademark Office file of the above-entitled application.

Respectfully submitted,

Frampton E. Ellis

60418177 - 101600

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STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) & 1.27(b))—INDEPENDENT INVENTOR	Docket Number (Optional)

Applicant, Patentee, or Identifier: Frampton E. ELLIS, III

Application or Patent No.: —

Filed or Issued: —

Title: Global Network Computers

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- [X] the specification filed herewith with title as listed above.
- [ ] the application identified above.
- [ ] the patent identified above.

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Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- [X] No such person, concern, or organization exists.
- [ ] Each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern, or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

Frampton E. ELLIS III		
NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
Signature of inventor	Signature of inventor	Signature of inventor
Date 8/25/00	Date	Date

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